Chips Act: the Chips for Europe Initiative

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European Conference on EDGE AI Technologies and Applications

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The EU Chips Act - rationale for intervention

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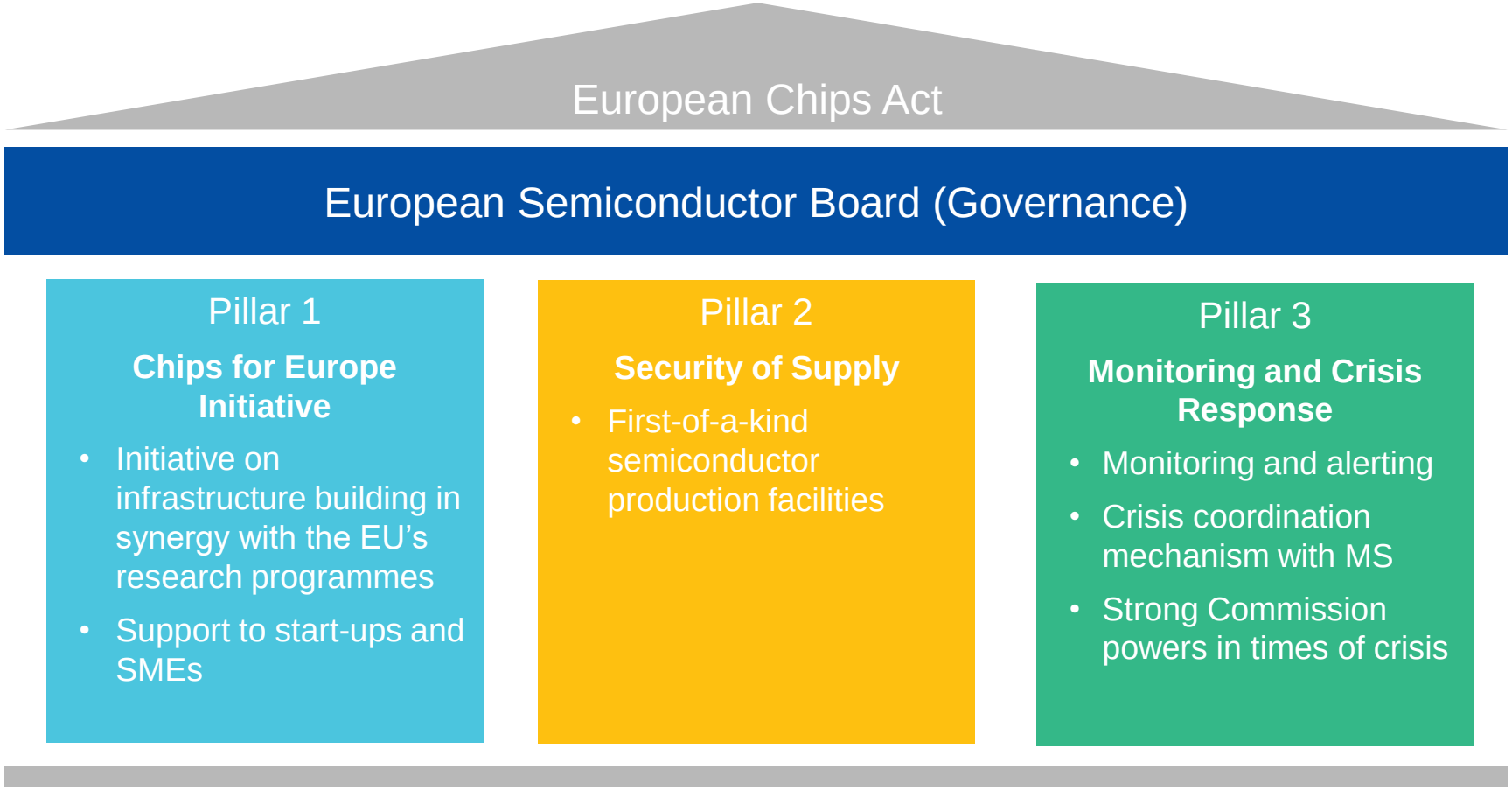
The Three Pillars of the Chips Act



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Chips for Europe Initiative

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Chips for Europe Initiative

Problem statement

- The EU's research programmes have largely not driven the conversion of its excellent research results into industrial innovation
- SMEs and start-ups have difficulty attracting the necessary investment
- The EU has a limited pool of talent and lacks a workforce with the necessary skills

Measures to help **bridge the gap to market** are required

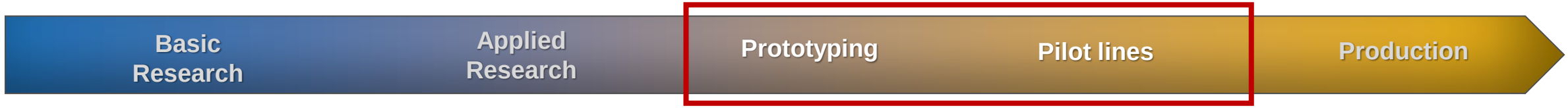
Chips for Europe Initiative
Aim: bridging the gap from lab to fab

5 Objectives

1. Reinforce design capacity by providing a **virtual design platform**
2. Enhance existing and developing new **pilot lines**
3. Accelerate the development of **quantum chips**
4. Expand **skills** and set up a network of **competence centres**
5. Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC
I-EU



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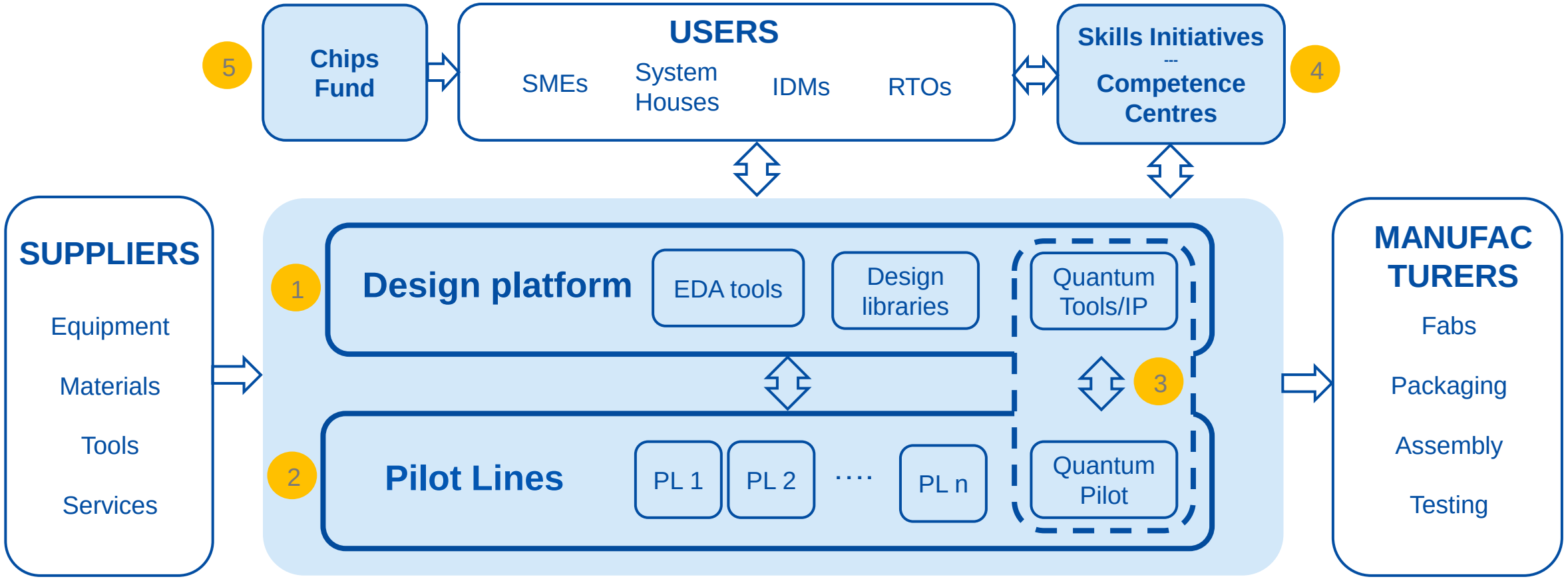
Chips for Europe Initiative
Bridging the gap from lab to fab



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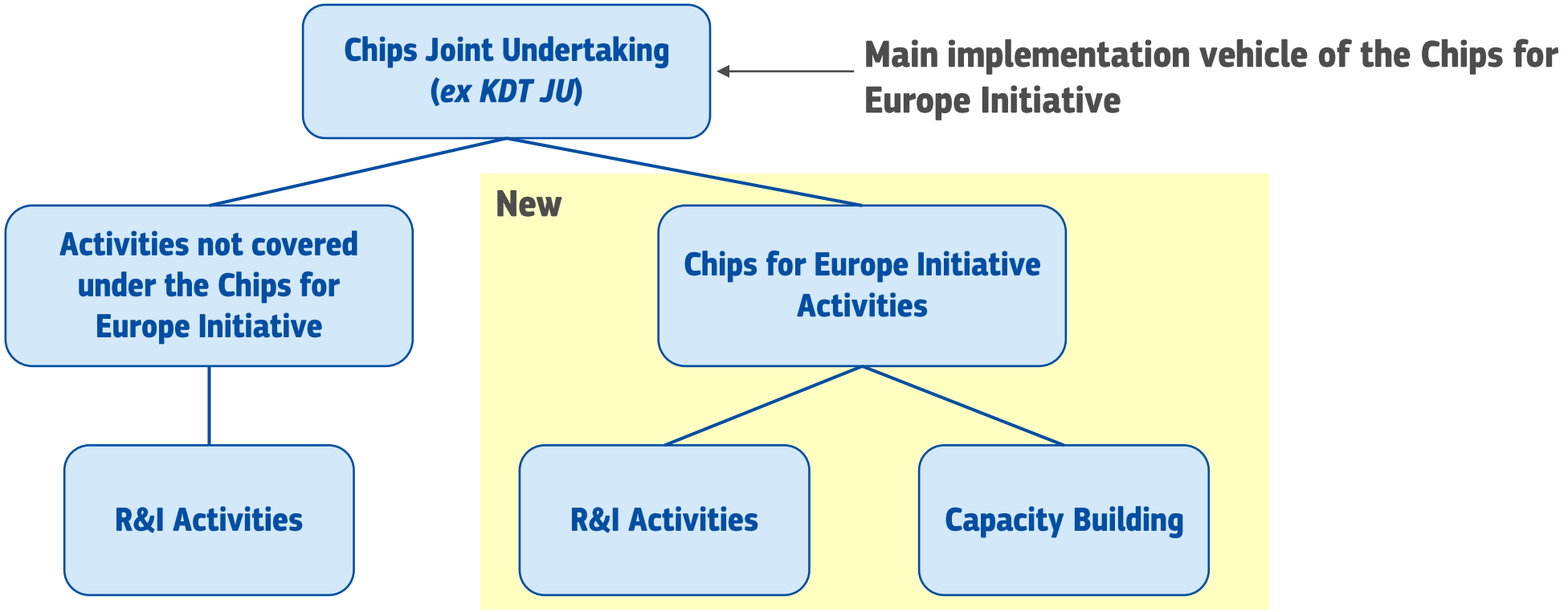
Chips JU Activities
Chips for Europe Initiative



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Pilot Lines

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Pilot Lines
Aims

- Provide users a common, state-of-the-art European test, experimentation and validation infrastructure accessible to a broad user base
- Contribute to the strengthening the security of supply and the semiconductor ecosystem in the Union
- Enable users to venture to new technology domains and support them in engaging in risky cutting-edge, next generation development

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Pilot Lines

Take aways from consultation workshops

Essential Elements

- Leading-edge technologies
- Industrial relevance
- In line with end-user requirements
- Industrialisation plans
- Pan-European

Models for implementation

- Development of process technology
- Service provision – “*pilot lines as a service*”
- Test and experimentation facilities
- In line with technology roadmaps

Access conditions

- Open to all
- Non-discriminatory
- Cost-efficient for users

Spill-overs

- Skills - pilot lines can serve as a tool for on-the-job training
- Consolidation and expansion of Europe’s ecosystem

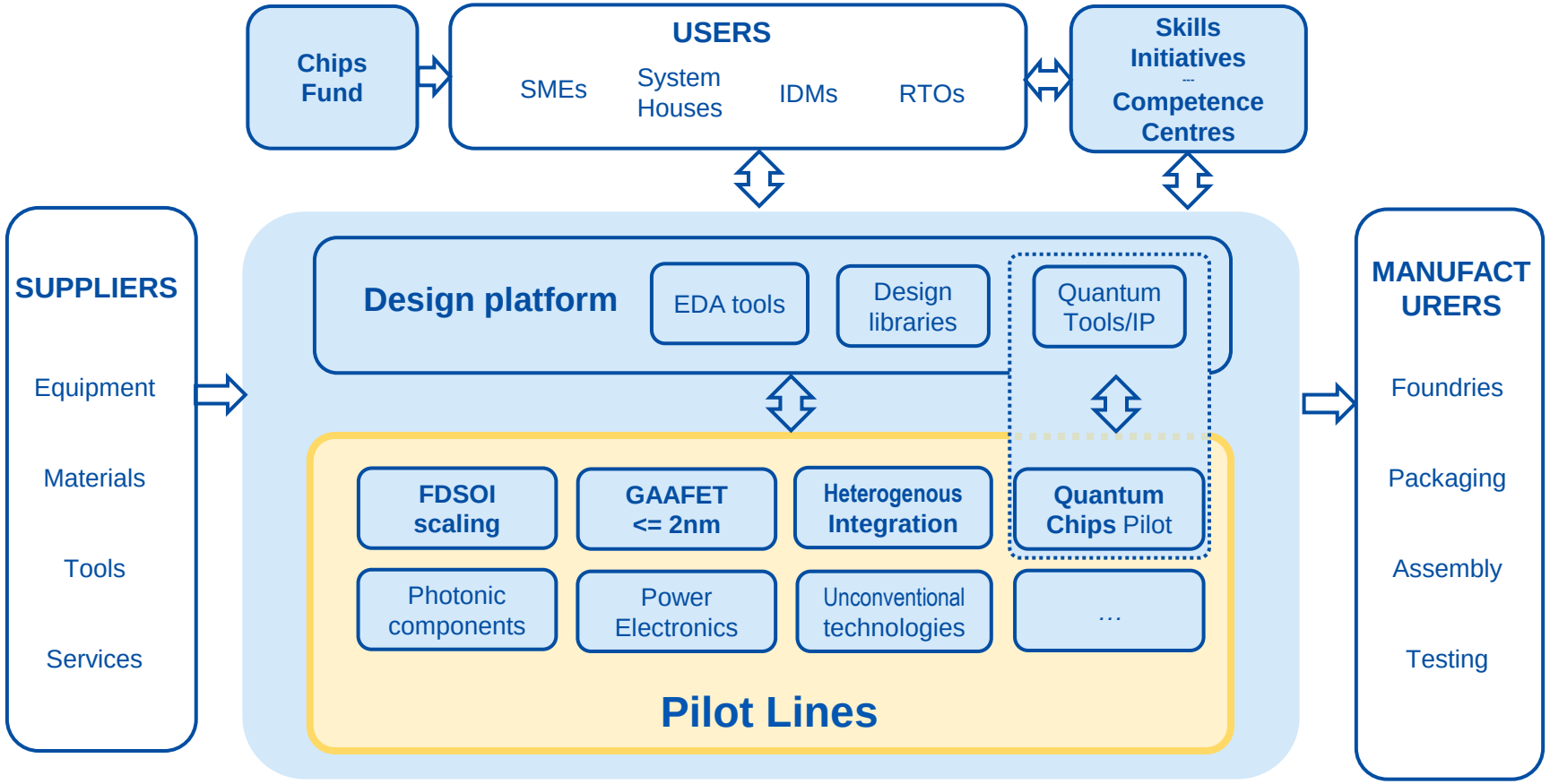
Pilot Lines in the Chips Act

Pilot Line Infrastructure

- *FD-SOI down to 10nm and below*
- *Leading-edge process at 2nm and below*
- *Advanced Heterogeneous System Integration*

Other technologies:

- *Quantum*
- Photonic
- Power, RF
- …



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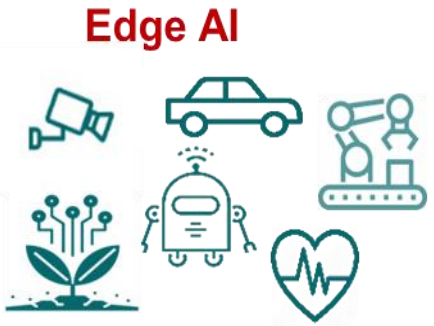
Testing & Experimentation Facilities for **Edge AI** hardware



PREV AI L

European platform enabling companies of any size to validate high-performance, low-power edge AI components and technologies

- Major initiative of **Digital Europe** Programme, heralding the concept of open EU pilot lines of the Chips Act, which will also build upon and harness this partnership
- The consortium includes four major European **RTOs** (CEA-Leti, imec, Fraunhofer, and VTT) that will leverage upon their 300mm facilities in a coordinated and complementary fashion
- This multi-hub platform will bring cutting-edge technologies to a higher maturity level and give users the possibility to fabricate and test edge **AI prototypes** based on innovative technologies:
  - Advanced non-volatile embedded memories (MRAM, OxRAM, FeRAM)
  - 3D heterogeneous integration and assembling (die-to-die, die-to-wafer, die-to-substrate, wafer-to-wafer)
  - Integrated photonics and RF components

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Competence Centre / Skills

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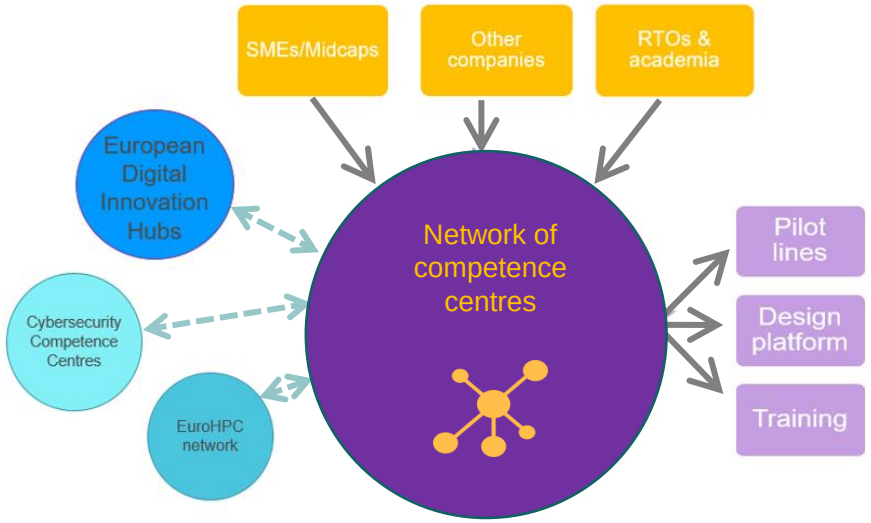
EU Network of Competence centers



Role of competence center

- Act as reference for own area of **expertise** and access point to network, matching **user needs** with available expertise
- Address skills shortage providing access to **training**, including up/re-skilling
- Facilitate access to **design platform** and **pilot lines**
- Support technology **transfer**
- Raising **awareness** on international programmes, promoting **services**, **funding** opportunities

EU Network of Competence centers

- Member States designate candidates
- Single organisation or coordinated group with complementary expertise
- No profit organisation (RTOs, Uni's)

- Synergies with EDIHs, can become CCs
- Governance autonomy, in line with objectives of the Initiative

EU support for at least one centre per Member State

Co-investment with Member States and Regions

Supporting industry and public services

Access to design platform and pilot lines

Focus on Semiconductors Skills

A strong European network of Competence Centres

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Skills – foreseen actions

Chips JU dedicated calls, in collaboration with Member States, for:

- Public awareness campaigns
- Scholarships and Traineeships
- Free training, upskilling and reskilling programmes
- Complementary mobility (Erasmus+)

Increase **visibility** of the semiconductor industry at early stages of education

Create a **mapping** of the skills needs from industry

Promote **gender equality** in the semiconductor industry

Up-skilling and **re-skilling** of the workforce.

Provide **support** for Higher Education and VET institutions.

Enable **cooperation** amongst all the relevant entities incl. Competence Centres

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Chips for Europe Initiative

Chips Fund

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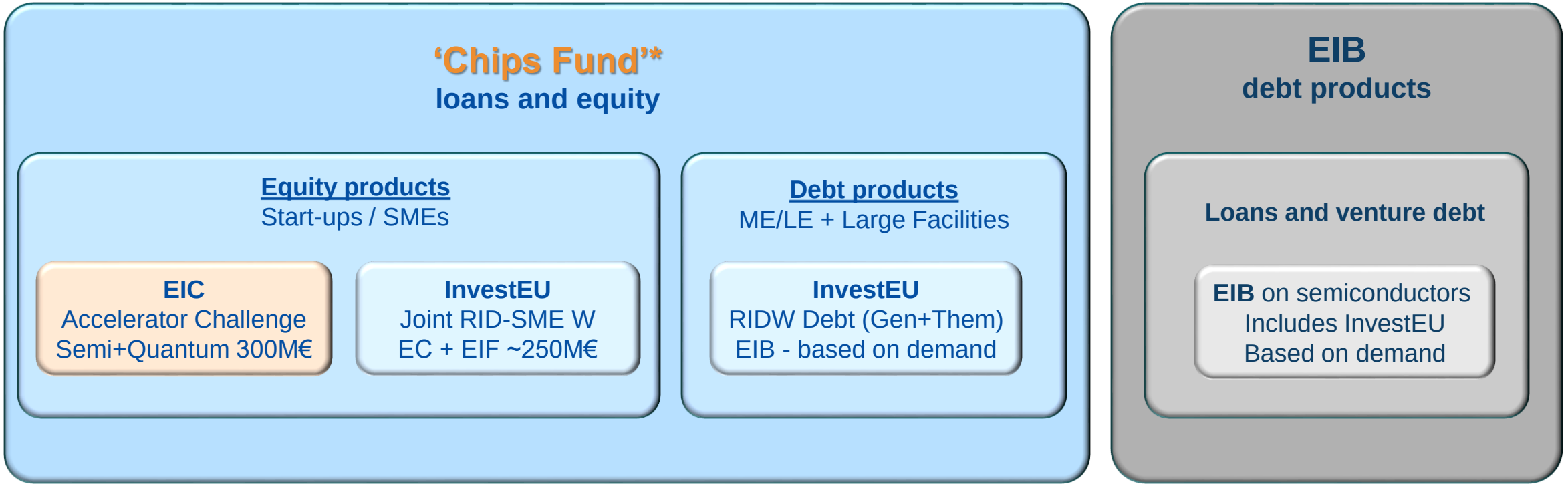
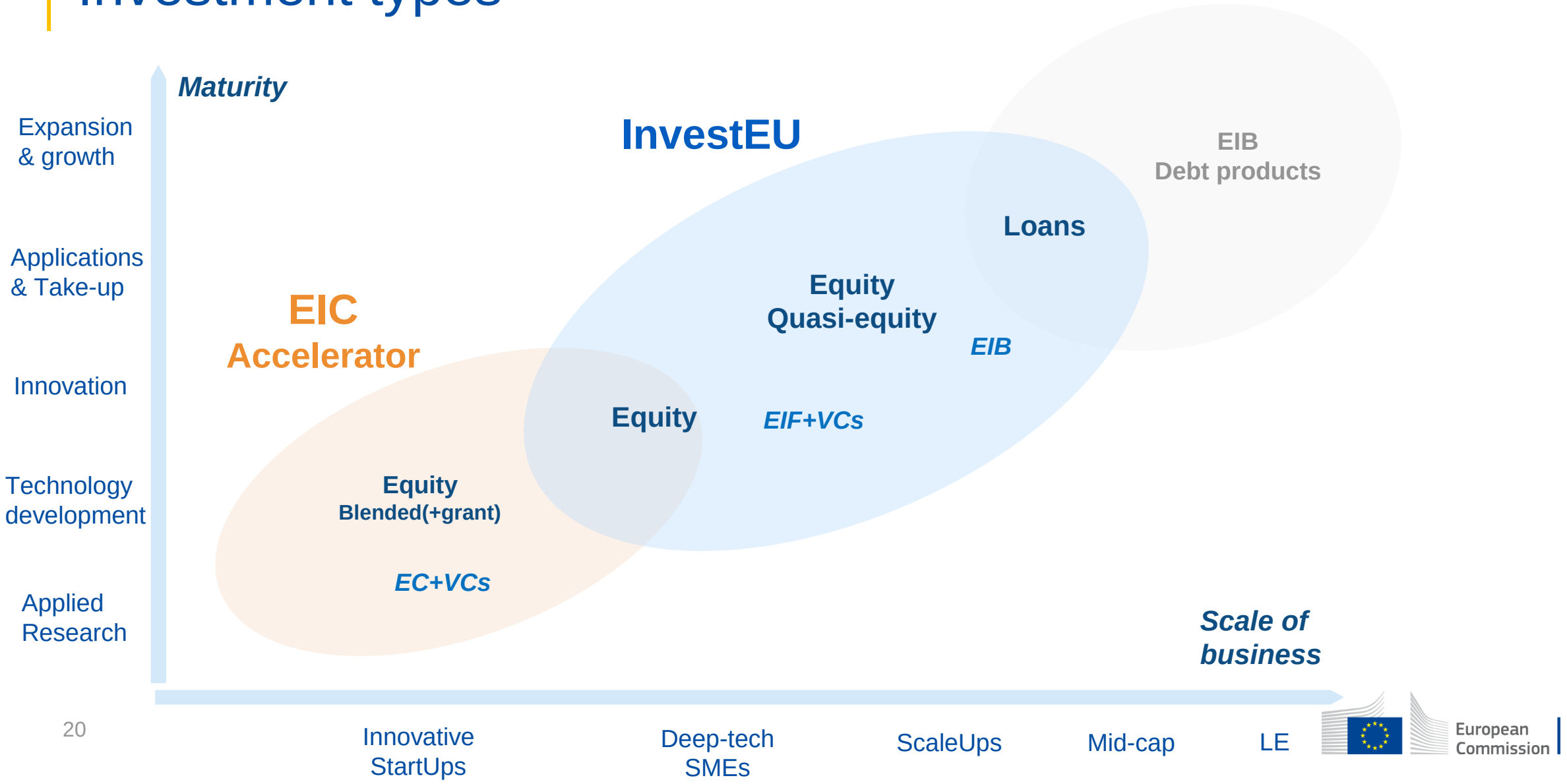
The “Chips fund” investment facility



* The “Chips Fund” will be implemented through an investment facility
Fund and eligibility criteria are in current EIB group mandates

Chips Fund
Investment types



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Chips for Europe Initiative
Design Platform

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Design platform - scope

Main objectives

- **Reduce entry barriers** and admin burden for EU companies engaging in chip design
- **Facilitate access** to pilot lines and foundries
- Foster **collaboration** among EU stakeholders, also on new IP and tools (incl. open-source, quantum)
- **Access** to network of **competence centers** offering **training** and support to boost design skills

Instrument

Develop a **virtual design platform,** offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

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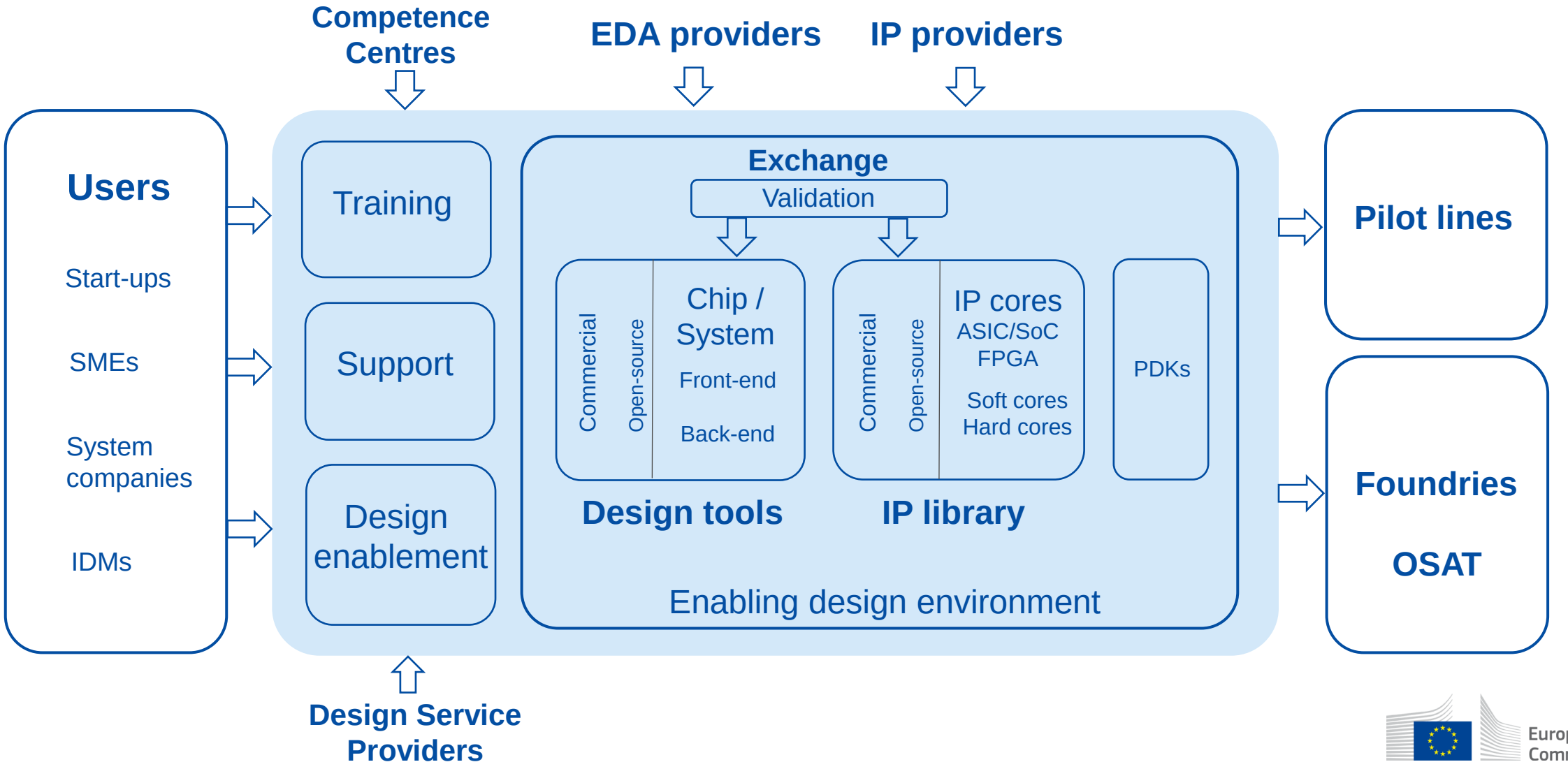
Design platform



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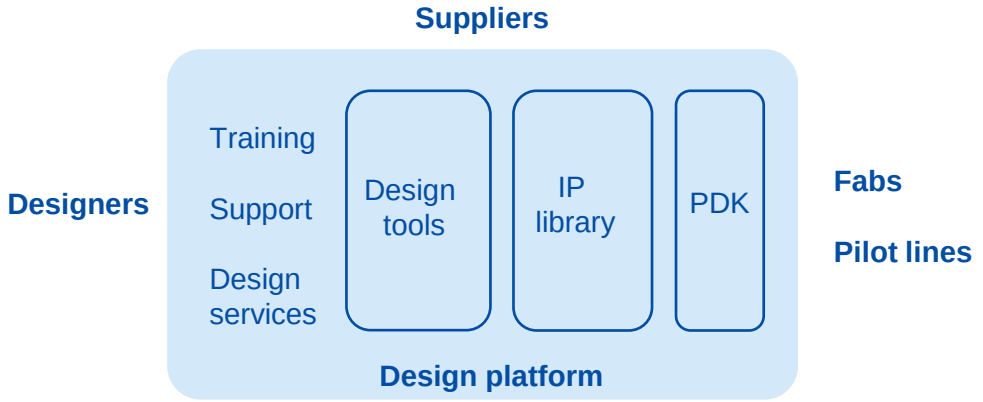
Design platform
Model



Added value

- Easy access on the **cloud**
- No upfront CapEx for on-premise IT **infrastructure**
- Maximum computing **scalability** for simulation and verification
- High level of **security**, fully audited
- **Streamlined process** with framework agreements
- Access to **prototyping**, **MPW** and foundry services

Key partners

- **Foundries**, **IP** vendors, **EDA** and **infrastructure** providers - collaboration for **secure cloud** solution
- ASIC/SoC **design services** for design enablement, workflows
- **Competence centers** offering training to address **skills** gap

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Design Platform and Europractice

Europractice

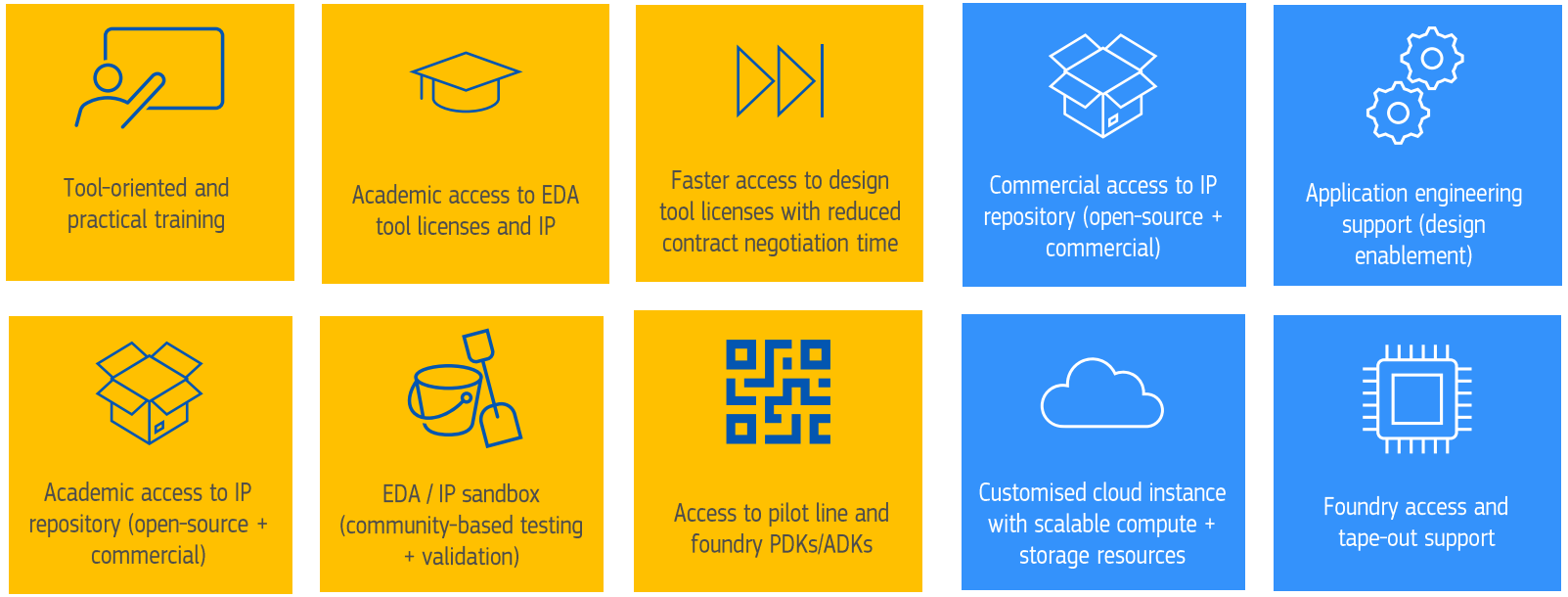
- **EU project** to stimulate microelectronics in **academia** and ensure supply of skilled engineers
- Established in 1989, it serves over 600 academic institutes with design **tools** and **MPW** runs for their teaching, research and innovation activities

European **Design Platform**

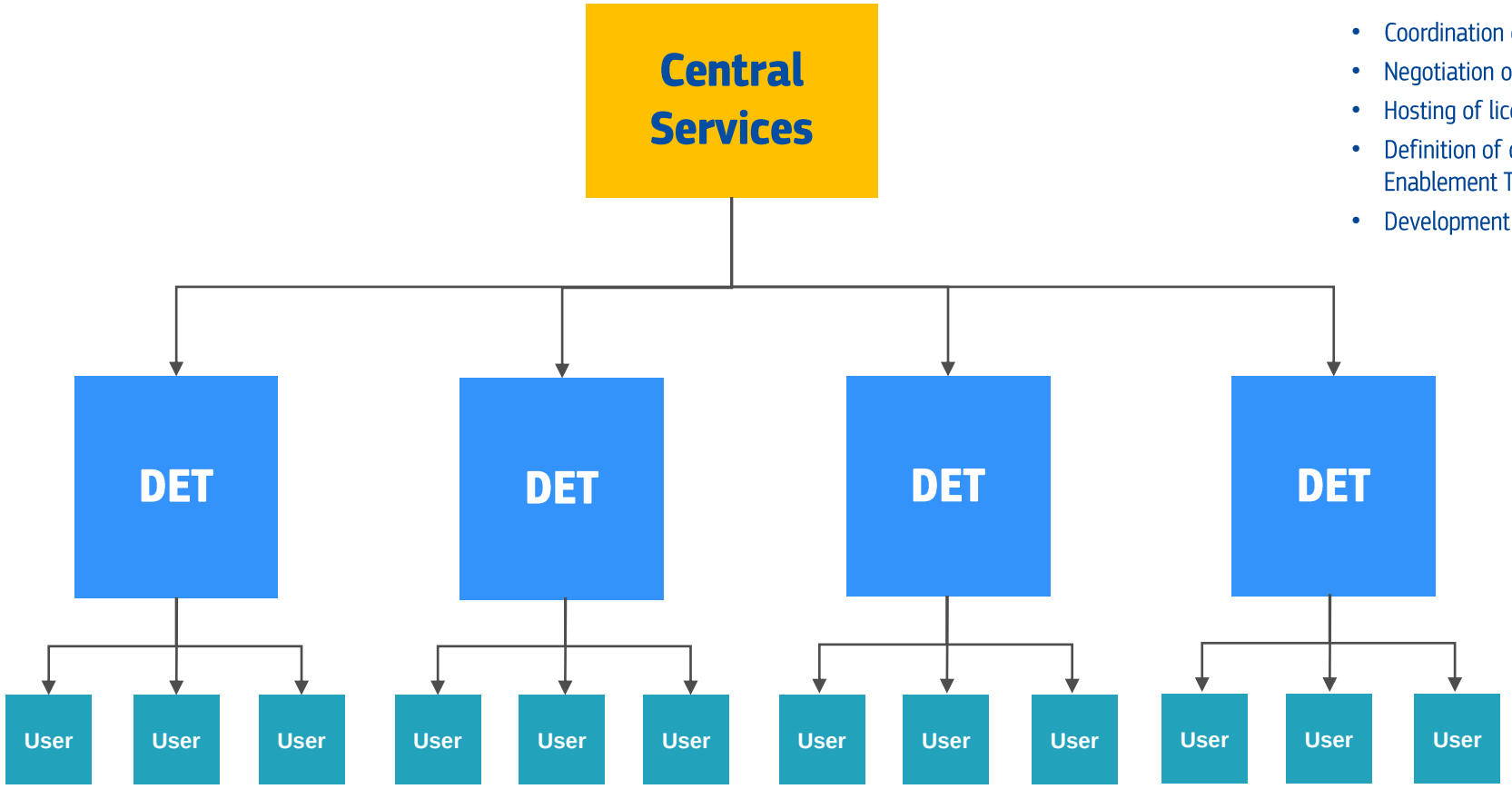
- Will focus on cloud-based access to commercial licenses of EDA tools and IP, offering design enablement services to EU/PS companies
- Targets support for fabless **SMEs**

A strong collaboration is envisaged between the 2 projects, and some services may merge to offer continuity among academia, spin-outs and industry at large

Services to be provided by the Design Platform



Design Platform Overview



Central services

- Coordination of the Design Platform
- Negotiation of framework agreements with vendors
- Hosting of licence server
- Definition of common look and feel across Design Enablement Teams (DETs)
- Development of Infrastructure as Code

Distributed services

- **Design Enablement Teams** with application engineering support to users
- Hosting of cloud instance
- Supporting users in setting up their design environment and design flows
- Interface with foundries for prototyping
- Supply chain management for prototypes and volume products
- Expert support for validation/characterization and qualification of IP and volume products

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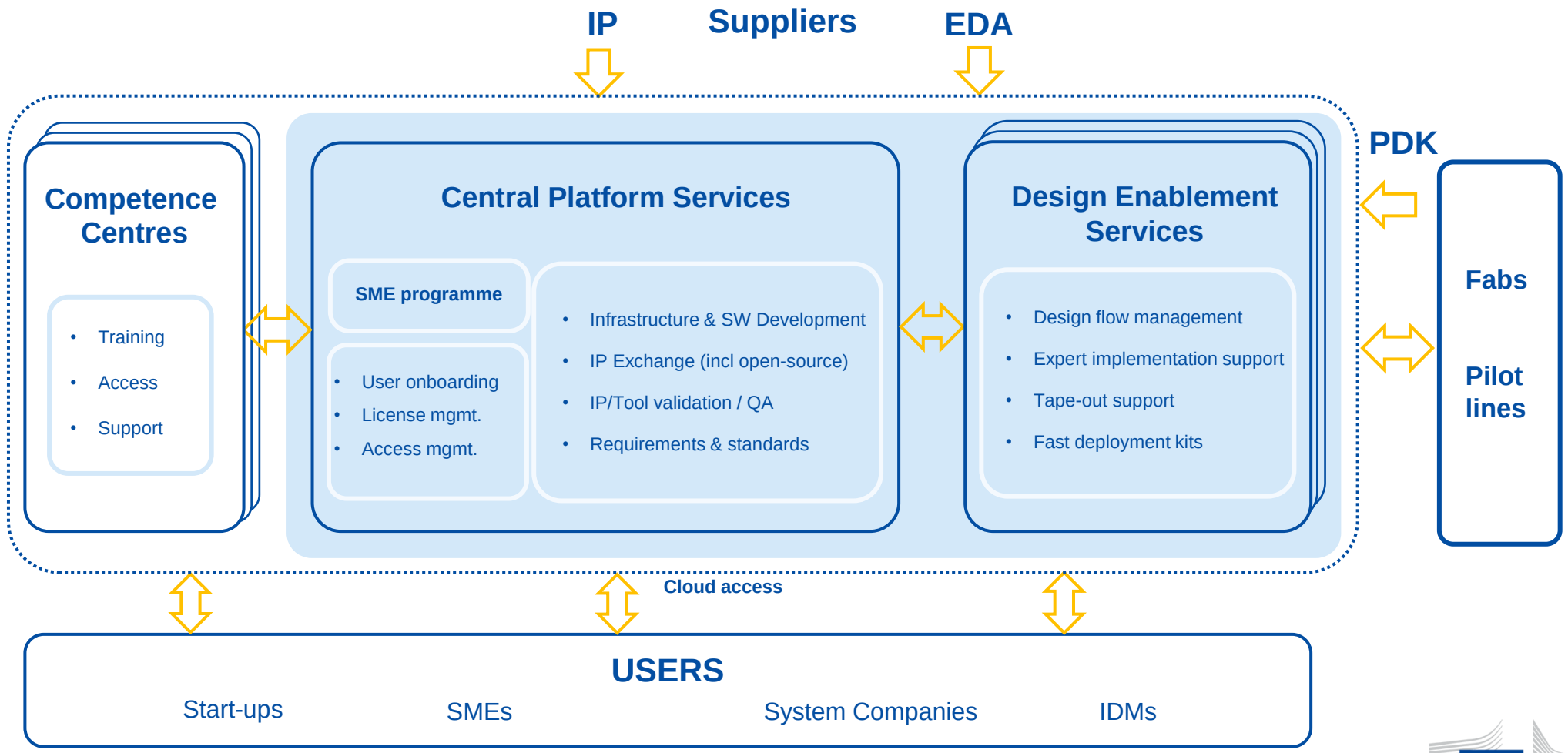
Design platform
Working Group Proposal



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Design platform for the design community

In addition to design, tape-out and training services, the platform aims to:

- Support collaborative **R&I projects** of Chips JU, in alignment with SRIA
- Offer a **community space** for designers to facilitate **collaboration** on precompetitive development and common design challenges, e.g.:

- IP exchange/repository
- Verification tools and methodologies
- Chiplet interfaces, modular design and integration
- Open source hardware
- Open-source EDA tools
- AI-based tools and solutions
- Edge-AI?… (you name it)

Design platform vs design R&I

Two parallel streams

Design platform services (C4EU Initiative)

- Aims to support EU design ecosystem
- Focused on operational objectives
- Could serve research and innovation
- Digital Europe + MS funding

Design research and innovation (ECS-SRIA)

- Innovation trough research projects focused on design challenges
- In higher TRLs can deliver innovation to DP
- Future fertilisation of the DP to ensure its evolution
- Horizon Europe +MS funding

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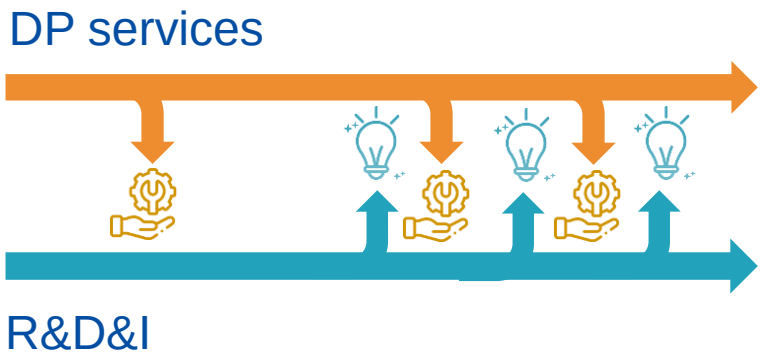
Chair ECS-SRIA



Edge AI can serve as enabler of advancements in semiconductor technology nodes, design approaches, and architectural innovations

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Thank you

Marco Ceccarelli

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