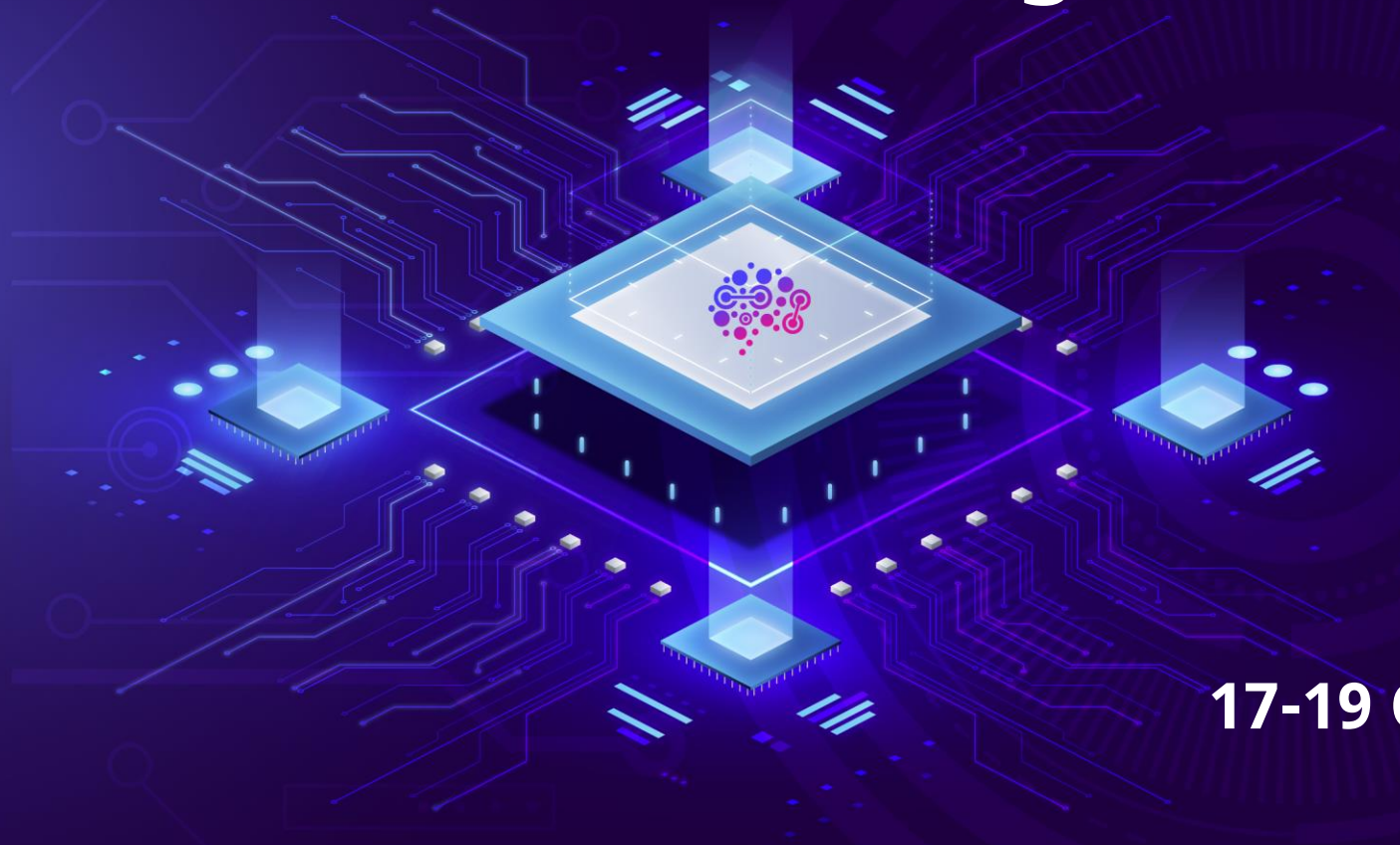
European Conference on EDGE AI Technologies and Applications - EEAI



Advancing emerging edge AI technologies and driving next generation intelligent applications.

17-19 October 2023, Athens, Greece

European Conference on EDGE AI Technologies and Applications - EEAI

PREVAIL project: Test and Experimentation Facility for the Realization and Validation of Prototype Chips Dedicated to Edge AI

Sergio Nicoletti, CEA-Leti, France

17-19 October 2023 Athens, Greece

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PREVAIL

www.prevail-project.eu

Funded by
the European Union

PREV AI L

A multi-hub Test and Experimentation Facility for edge AI Hardware

Funded by
the European Union

VISION

The **PREVAIL project** will establish and start operating the core of a networked, **300 mm** multi-hub **platform** to **provide chip fabrication capabilities** in advanced technology to EU stakeholders for **A**rtificial **I**ntelligence applications.

Funded by
the European Union

Few Numbers about Prevail

156	M€ Budget: ~ (50% funded by EC, 50% by State Members)
55	300 mm Tools procured via PREVAL
6	% (8.6 M€ & 342 pm) dedicated to Demonstrators Fabrication
3	Number PREVAIL Demonstrators:
	⇨Non-Volatile Memories
	⇨ 3D Assembly and Packaging
	⇨ Photonics/RF
2029	Last Year of operation of the PREVAIL Pilot Line
XX	Number PREVAIL Prototypes fabricated for the Edge AI community

- A dedicated Team to interface with the Users of the Pilot line

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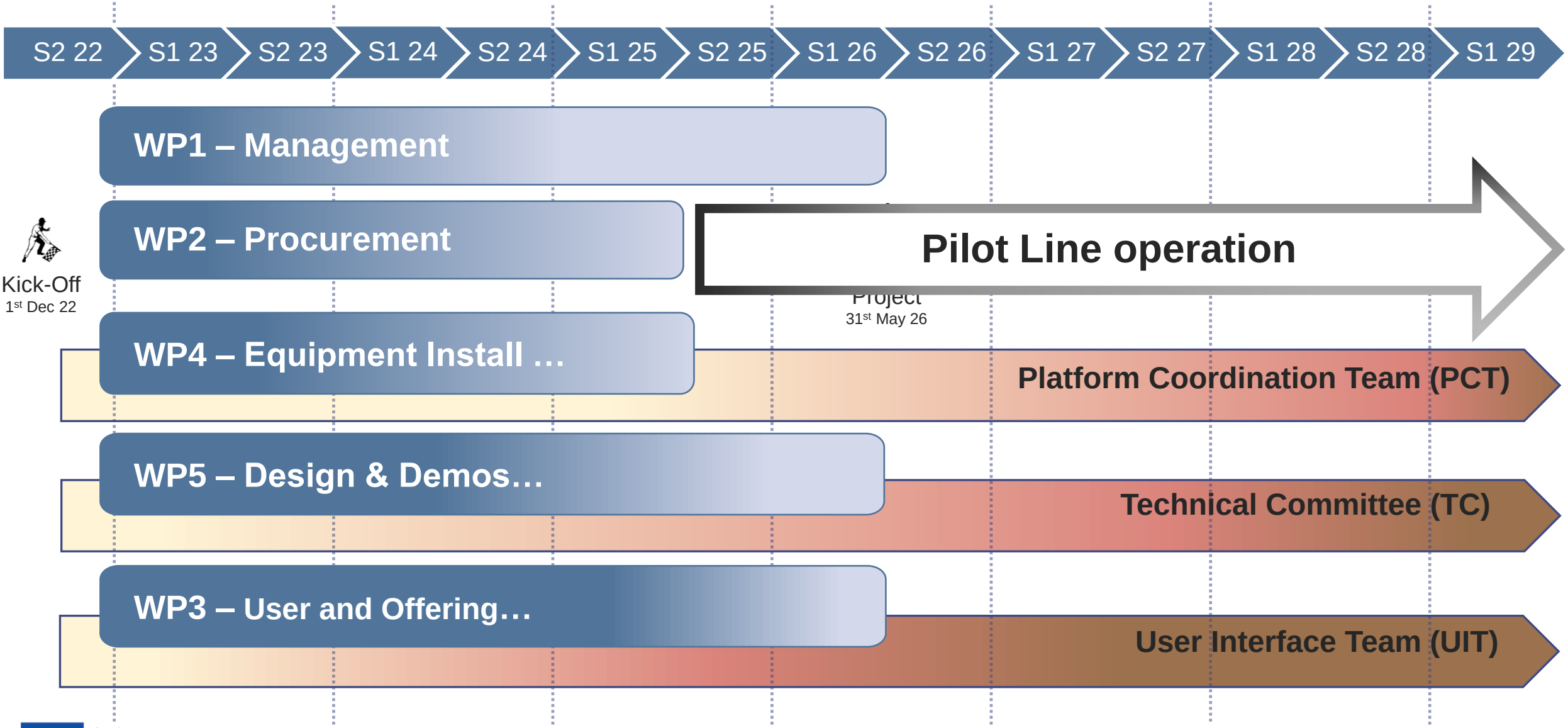
Timeline



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OFFER

Open access Pilot Line for edge AI chip prototyping

PREVAIL will enable a trusted **infrastructure** in **Europe** where companies and research institutions will be able to **fabricate** early **prototype** samples and test them in real **edge AI applications**.

Our offer will include the most promising technologies developed by the consortium partners to address the specifications required by edge AI chips.

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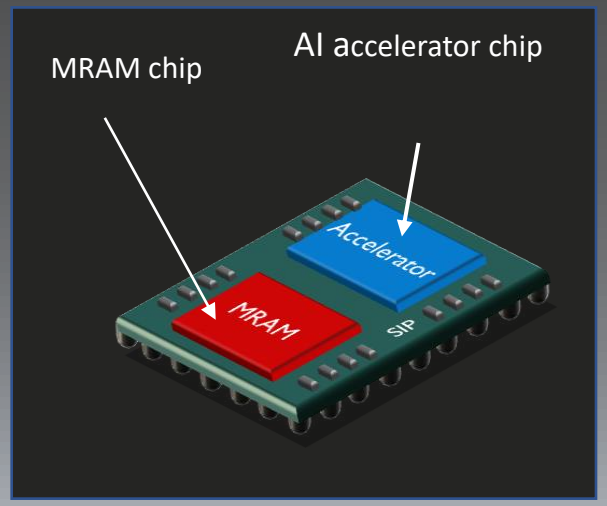
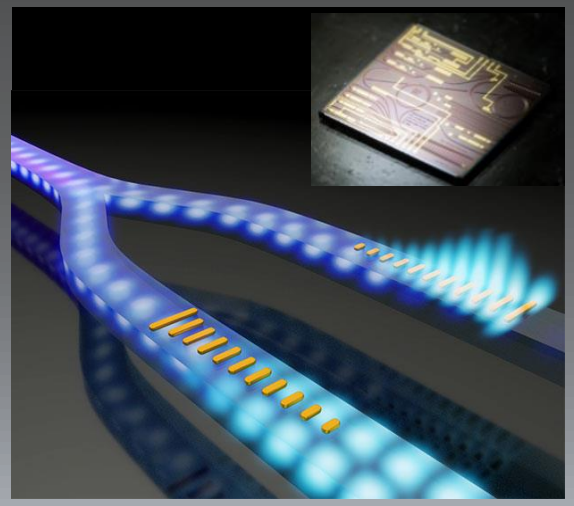
OFFER

Open access pilot line for edge AI chip prototyping

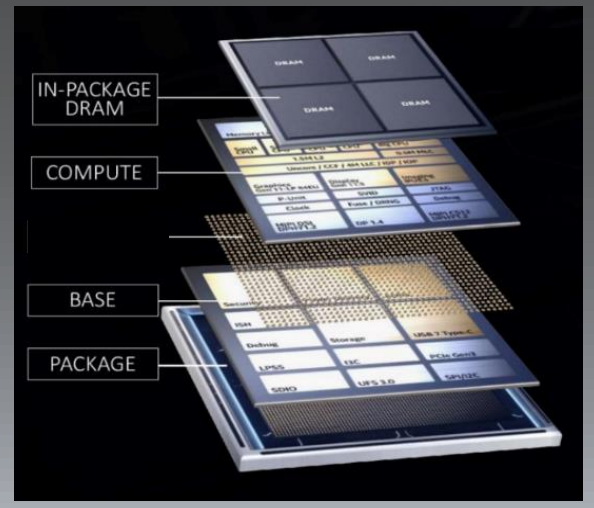
Non-Volatile Memories



Si Photonics



3Di Applications



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Technologies Overview

	non-volatile embedded memories			3D heterogeneous integration and assembling			photonics and connectivity	
	MRAM	OxRAM	FeRAM	die to die	die to wafer	wafer to wafer	integrated photonics	RF
CEA		✓			✓	✓	✓	
imec	✓				✓	✓	✓	
FhG			✓ (IPMS, IIS)		✓ (EMFT)	✓ (IZM-ASSID)		
VTT				✓	✓			✓

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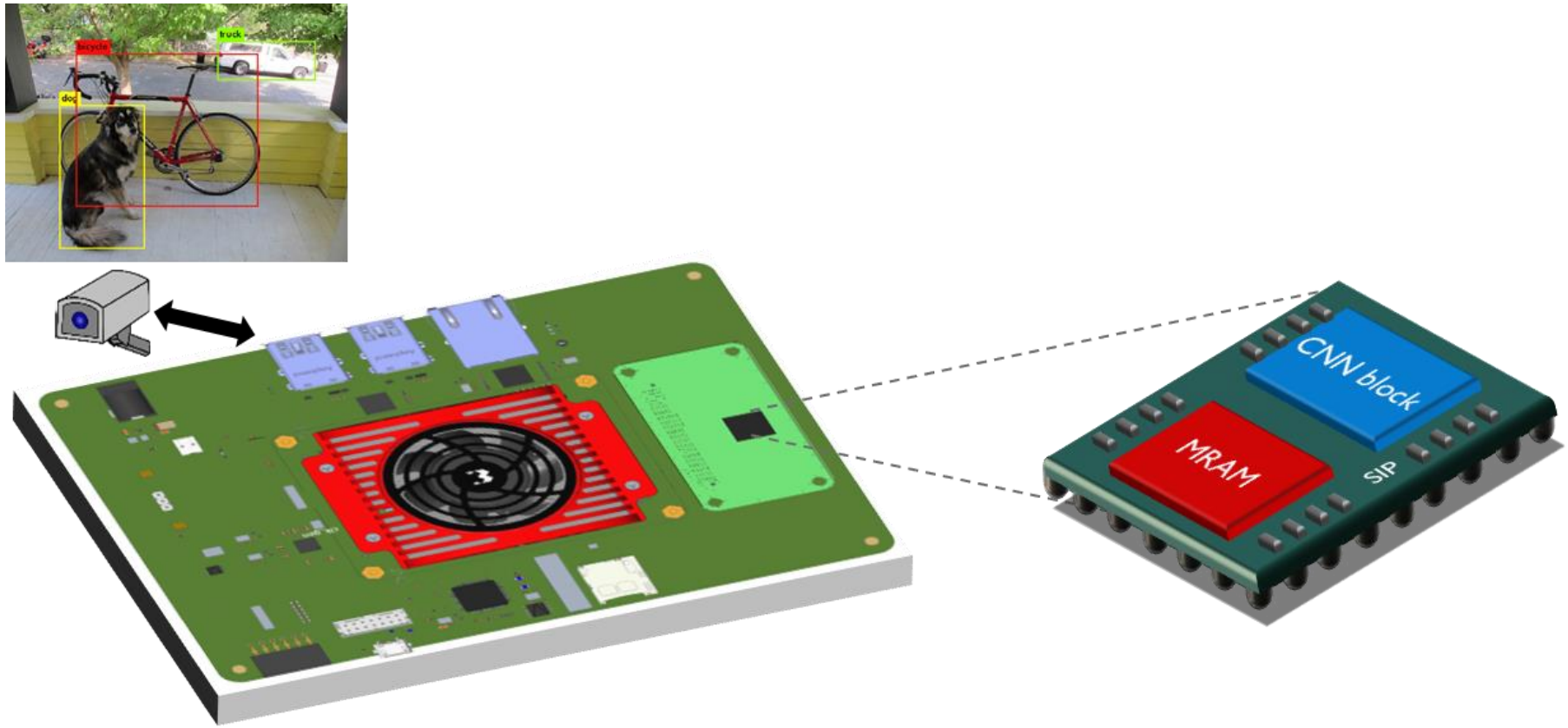
NVM Demo

Advanced analysis of Video captured by Smart camera; AI accelerator constantly analyses the motion, while Memory preserves the video history buffer to enable advanced processing



Technical DEMO definition: co-packaged of low-power low-latency AI accelerator with Advanced memory (MRAM)

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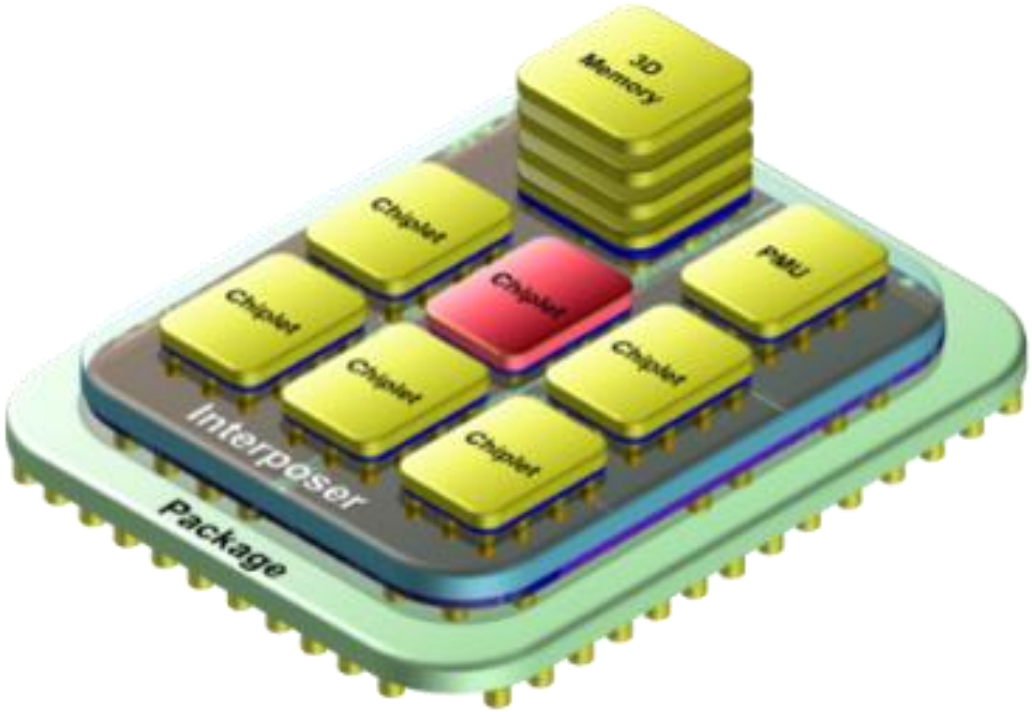
3D Demo

Vision: any chip on any interposer and any packaging for any application



- *Active and Passive Interposer*
- *TSV Last*
- *TSV Middle*
- *Low T Hybrid Bonding (< 200 °C)*
  - W2W
  - C2W
- *C2W High Density Hybrid Bonding*
- *µBumps*

Technical DEMO definition: 3D stacking of multiple chips on a single interposer mixing different enabling technologies

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Partnership for **Re**alization and **V**alidation of **AI** hardware **L**eadership

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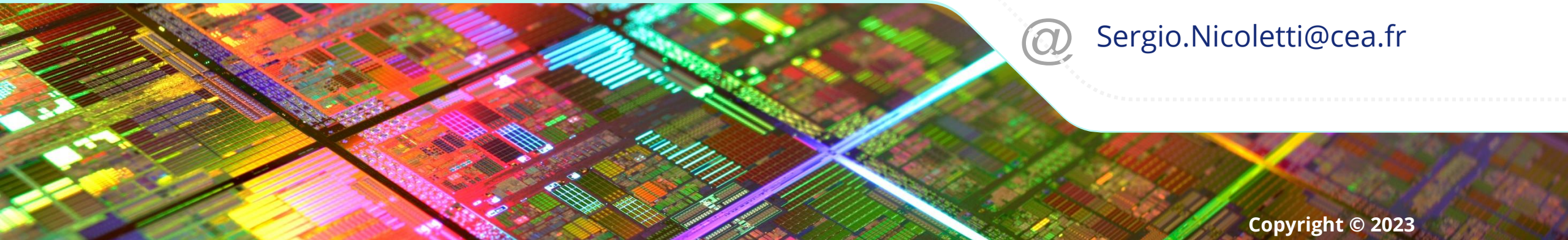
EDGE AI

Thank You

For your attention



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