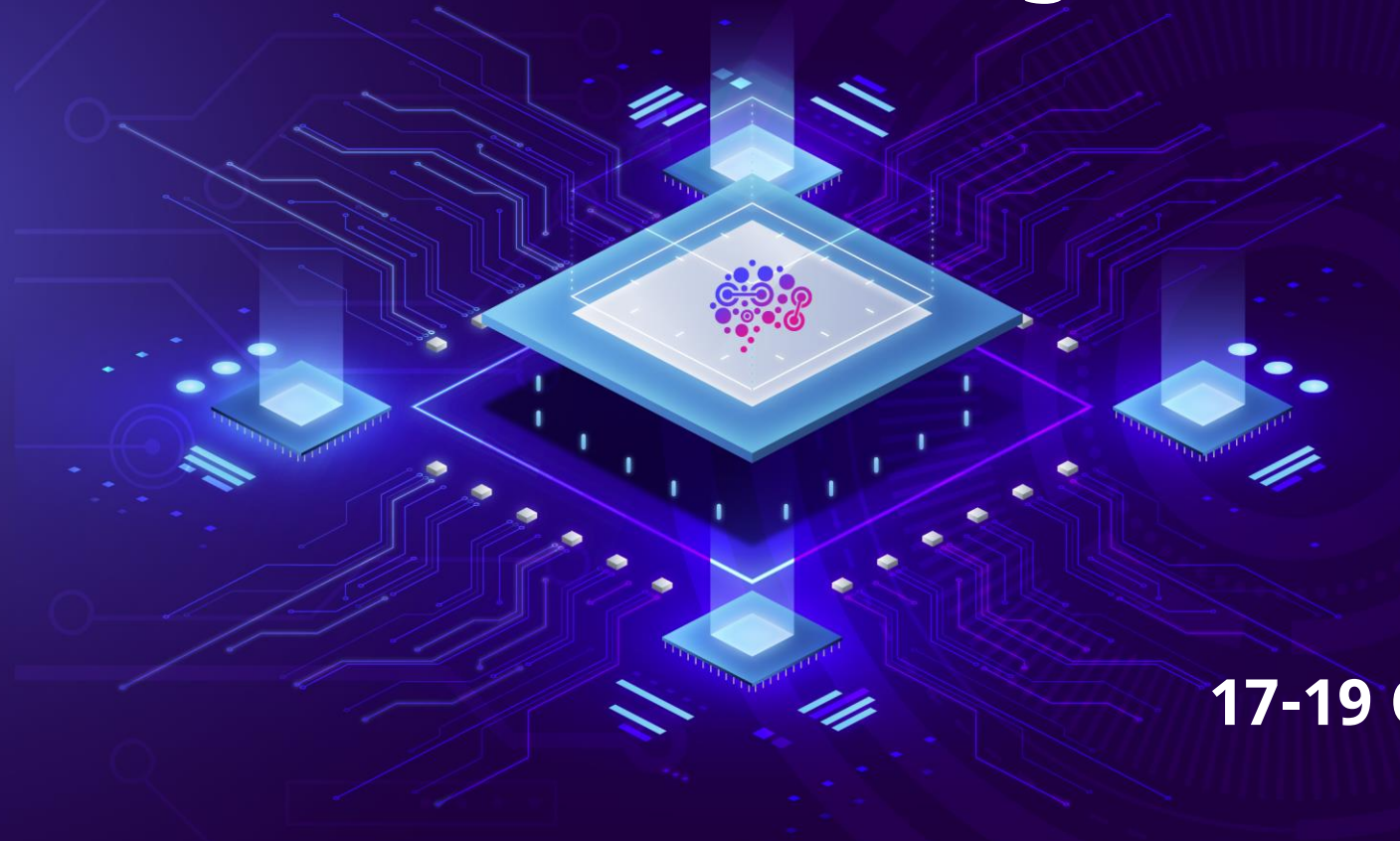
European Conference on EDGE AI Technologies and Applications - EEAI



Advancing emerging edge AI technologies and driving next generation intelligent applications.

17-19 October 2023, Athens, Greece

European Conference on EDGE AI Technologies and Applications - EEAI

(EU enabled) Technology initiatives converging to a massive edgeAI market

Gerardo Daalderop

NXP Semiconductors, the Netherlands

17-19 October 2023 Athens, Greece

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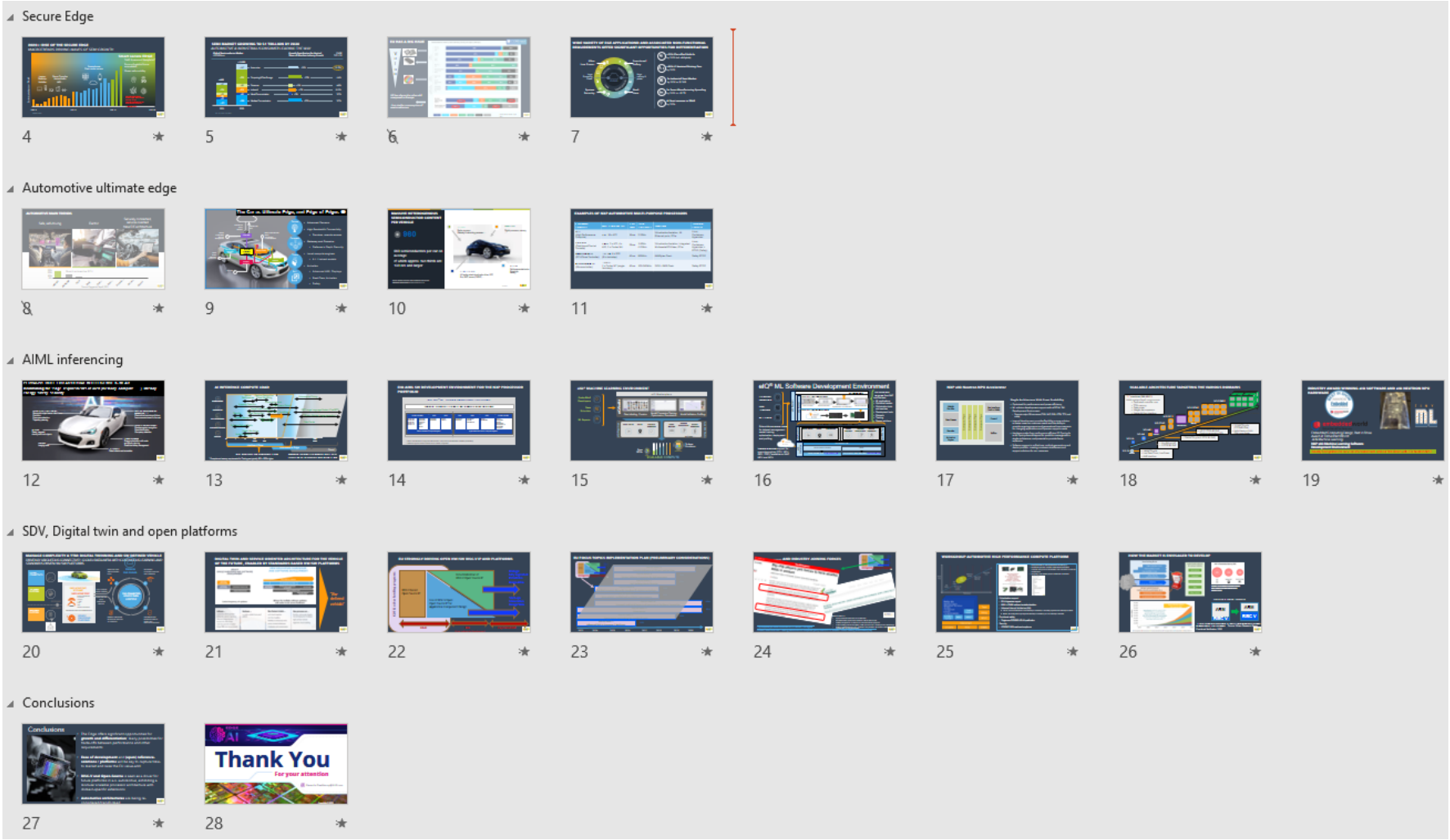
Presentation Outline

- Intro Secure edge
- Automotive the ultimate edge
- AIML inferencing
- SW defined vehicles, digital twin and open platforms
- Conclusions



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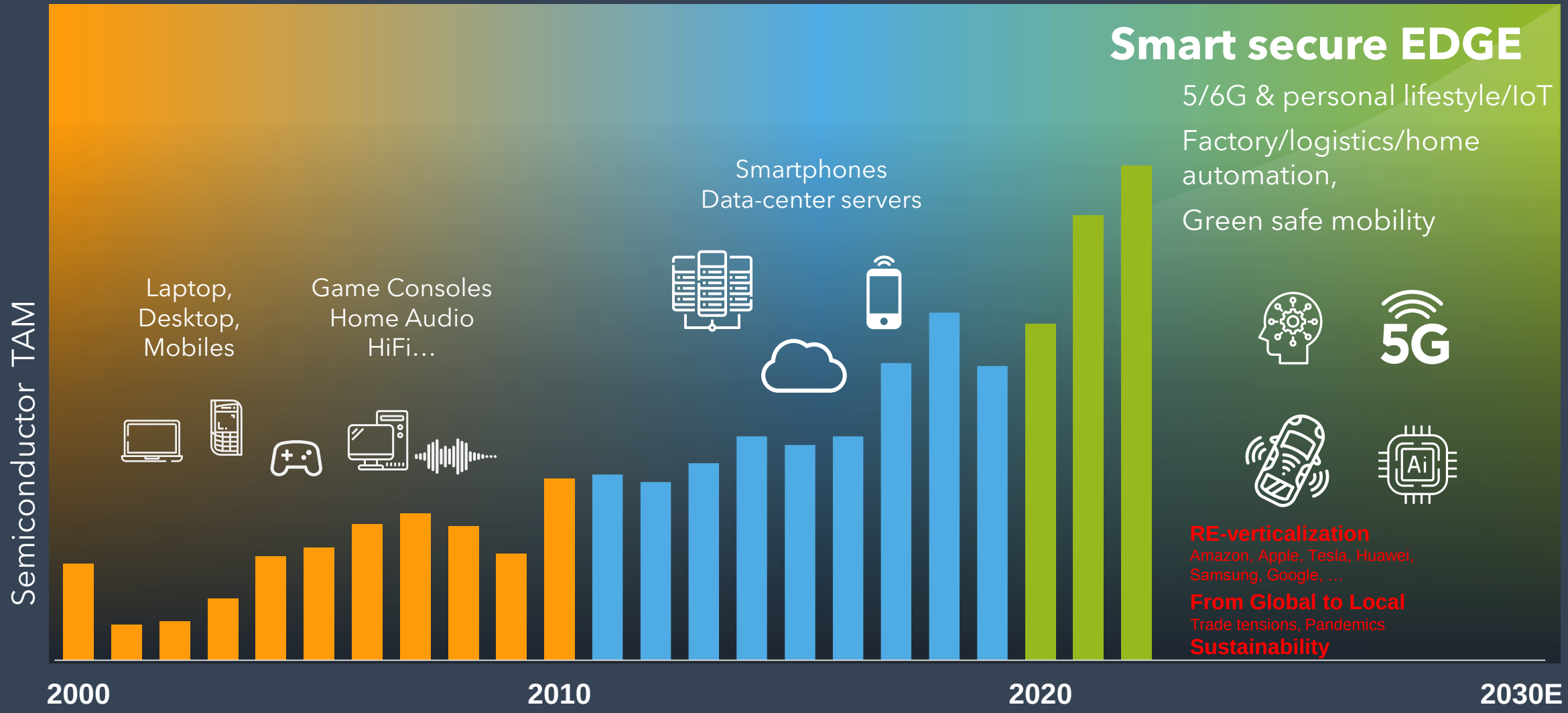
2020+: RISE OF THE SECURE EDGE

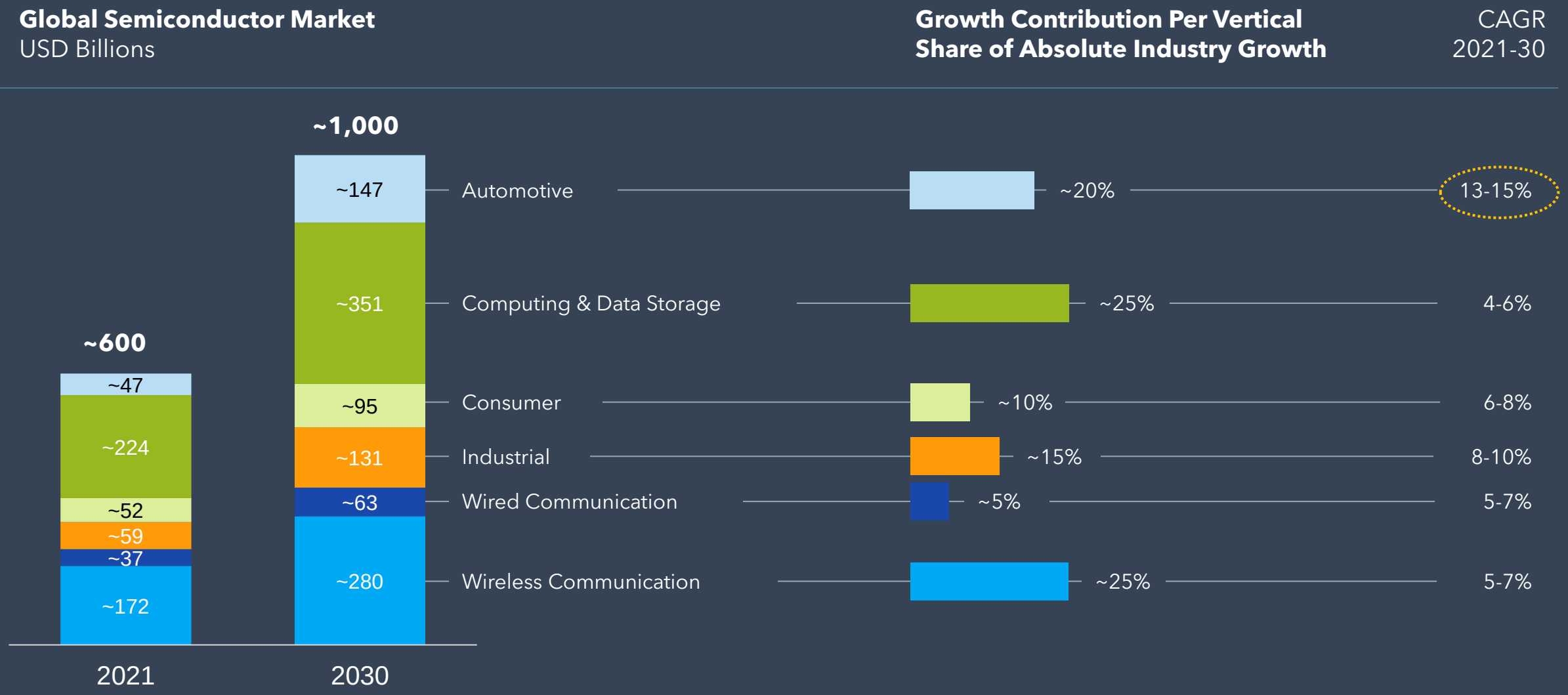
MACROTRENDS DRIVING WAVES OF SEMI GROWTH



Source: I.H.S.

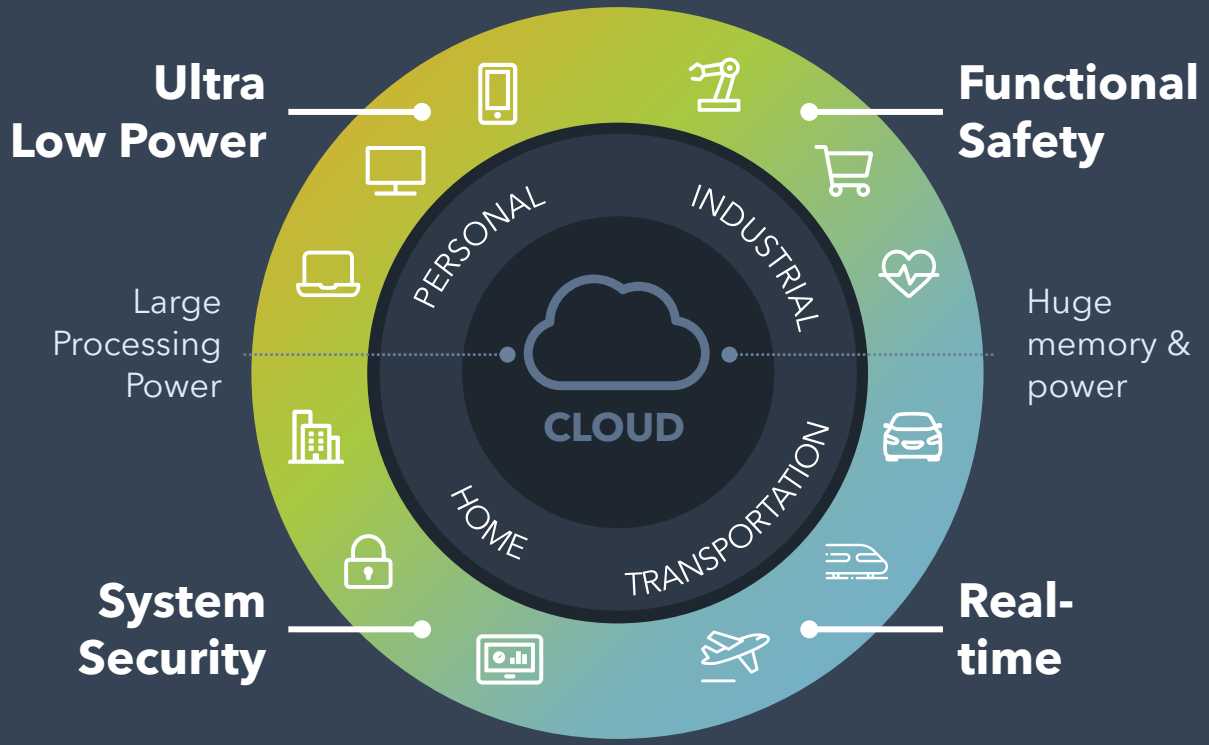
SEMI MARKET GROWING TO $1 TRILLION BY 2030

AUTOMOTIVE & INDUSTRIAL/CONSUMER LEADING THE WAY



Source: McKinsey 2022

WIDE VARIETY OF EGE APPLICATIOND AND ASSOCIATED NON-FUNCTIONAL REQUIREMENTS OFFER SIGNIFICANT OPPORTUNITIES FOR DIFFERENTIATION



>70% Electrified Vehicle
by 2030 (incl. mild hybrids)

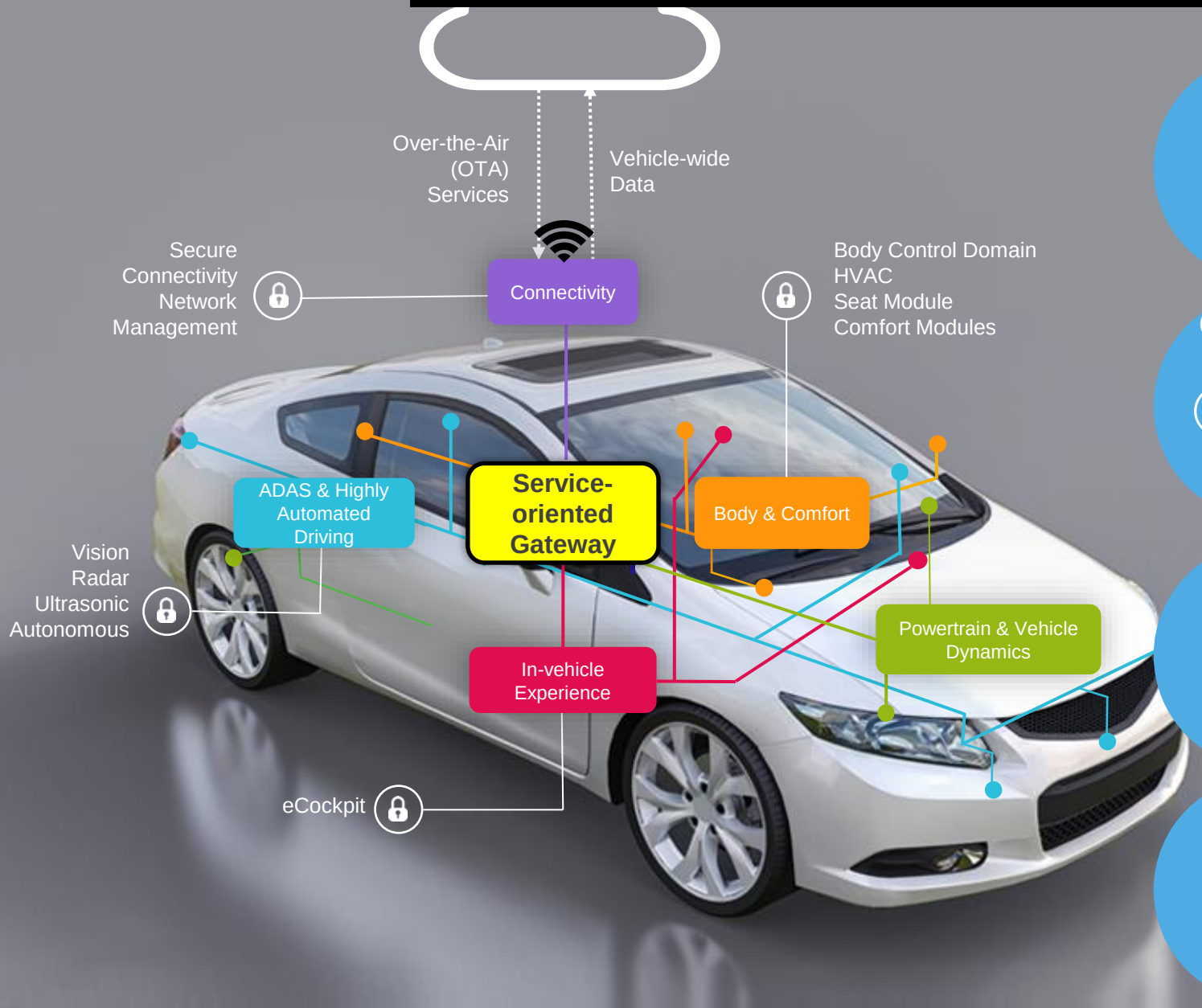
>50% L2 Assisted Driving Cars
by 2030

2x Industrial Semi Market
by 2030 to $130B

3x Smart Manufacturing Spending
by 2030 to ~$1T$

AI Semi revenue to $86B
by 2026

The Car as Ultimate Edge, and Edge-of-Edges ☺



Sense

Connect

Think

Act

- Advanced Sensors
- High Bandwidth Connectivity
  - Services, remote access
- Gateway and Domains
  - Defense in Depth Security
- Local compute engines
  - A.I. / trained models
- Actuation
  - Advanced HMI, Displays
  - Real-Time, Actuation
  - Safety

MASSIVE HETEROGENOUS SEMICONDUCTOR CONTENT PER VEHICLE

960

960 semiconductors per car on average

of which approx. two thirds are 130 nm and larger

16 nm
Radar processor
Gateway & networking processor ....

<=40 nm
Digital processors, memory
....

65 – 350 nm
HV analog mixed signal motor driver, LED,
Bus, BMS, sensors, MEMS, ...

>1 µm
Performance electronics
Powertrain
Battery ....

Source: Strategy Analytics, ZVEI, statements from various companies Image source: Nerthuz/ Shutterstock.com

PUBLIC

EXAMPLES OF NXP AUTOMOTIVE MULTI-PURPOSE PROCESSORS

Processor Category	NXP Example SoC	Process	Core Frequency	Features	Software Platform
HPC (High Performance Compute)	**LX2:** 16 x A72	16nm	2.2GHz	Virtualization/Isolation, 16 Ethernet ports, PCIe	Linux, Containers, Hypervisor
E-cockpit (Dashboard/Central Console)	**i.MX8:** 2 x A72, 4 x A53, 2 x Cortex M4	28nm	1.6GHz /1.2GHz	Virtualization/Isolation, Integrated Multimedia/3D/Video, PCIe	Linux, Containers, Hypervisor + RTOS (Safety)
Real-Time MCU (ECU/Zone Controller)	**S32S24:** 4 x R52 (8 in lockstep)	40nm	800MHz	64MBytes Flash	Safety RTOS
Automotive MCU (Microcontroller)	**S32K35:** 1 x Cortex M7 (single /lockstep)	40nm	120-240MHz	512K - 8MB Flash	Safety RTOS

PERVASIVE ROLE FOR ARTIFICIAL INTELLIGENCE IS NEAR

maintaining the ‘edge’ requirements of cost (memory, compute, ….), latency, energy, safety, security….

DRIVER REPLACEMENT
Raw and/or object sensor data fusion
Prediction
Free space detection
Trajectory planning

VISION
Detect, segment,
classify and track objects

RADAR
Imaging radar

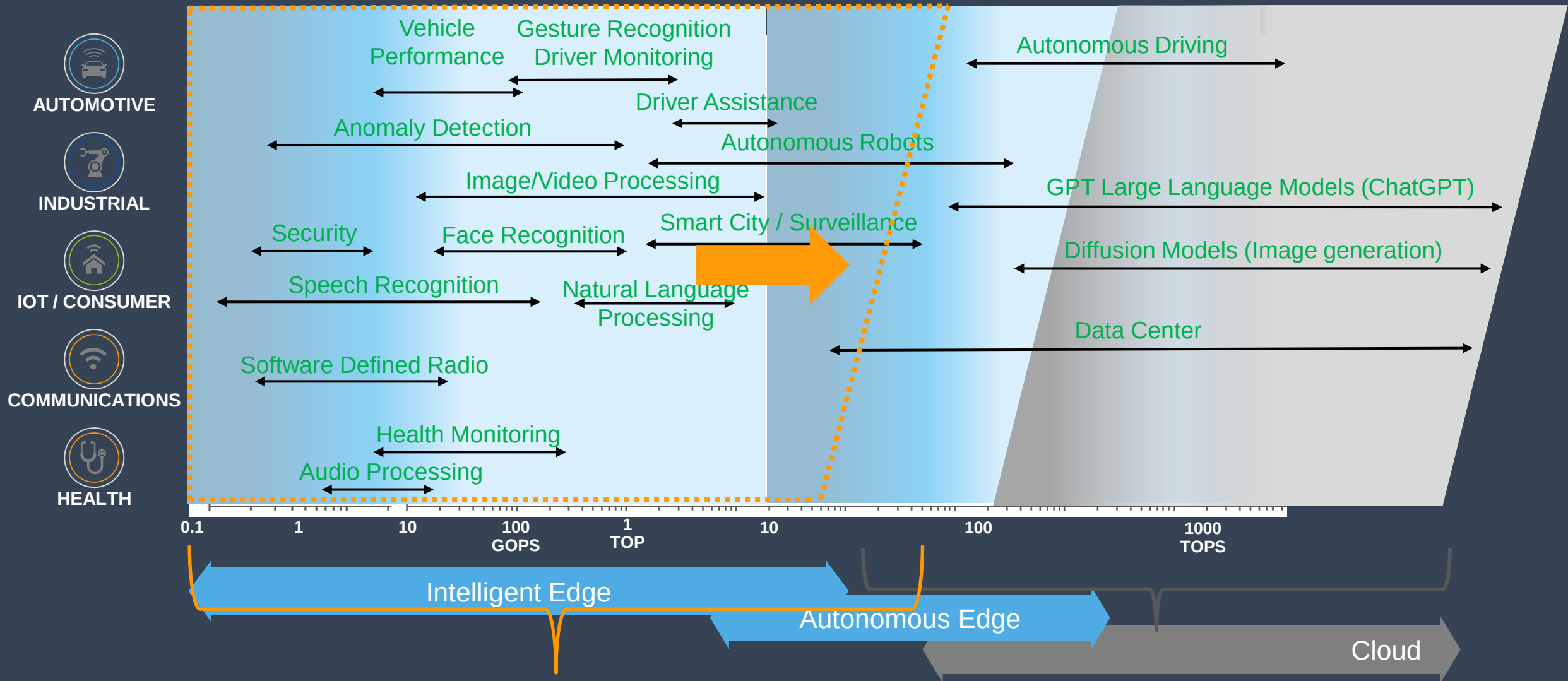
INTER-ENVIRONMENT AWARENESS
Personalized experience follows from one environment to the next

DRIVER MONITORING
Face/expression recognition
Face identification
Occupancy detection

POWERTRAIN
Energy optimization with route and terrain planning
Predictive battery management

SECURITY
Detect attacks and anomalies

AI INFERENCE COMPUTE LOAD

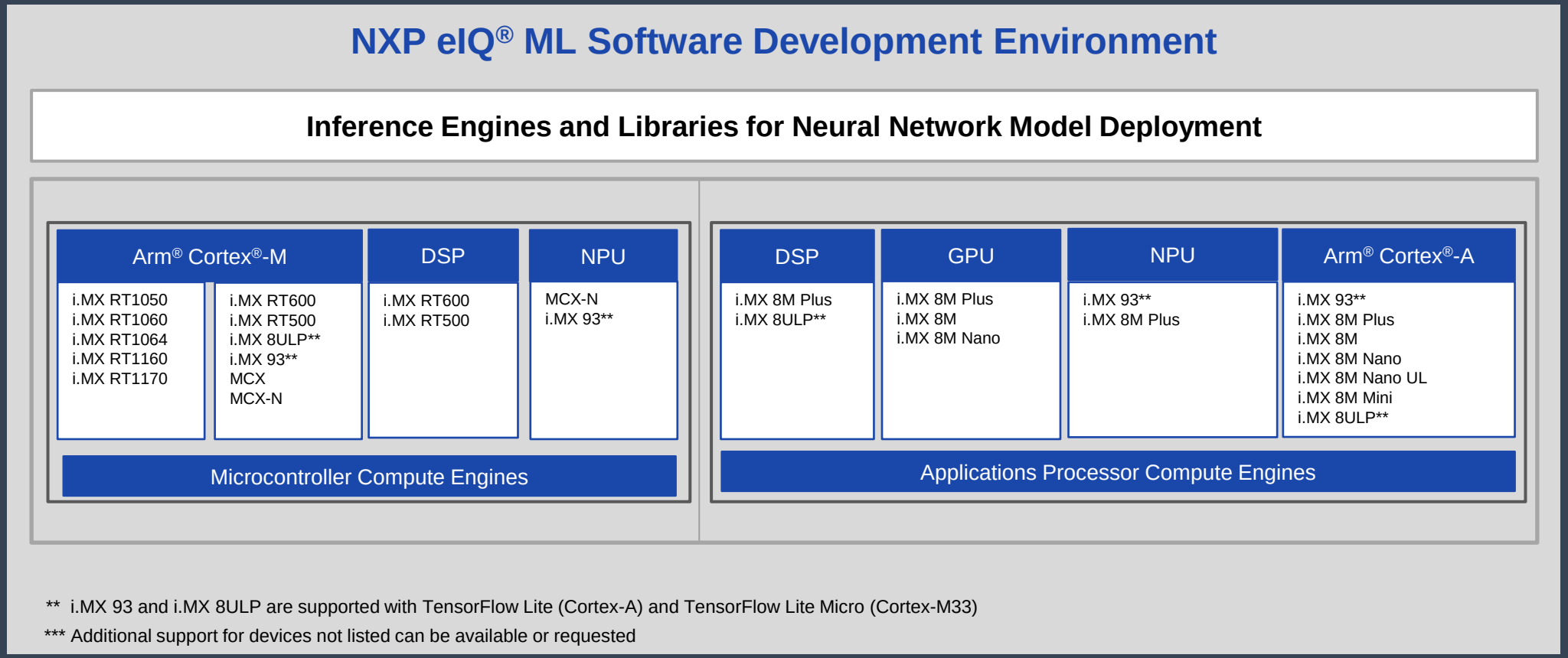


NXP enabling the Intelligent Edge

Massive parallel processing and cloud compute for autonomy and large LLMs

* Compute and memory requirements for Training are typically 100 – 1000x higher

EIQ AIML SW DEVELOPMENT ENVIRONMENT FOR THE NXP PROCESSOR PORTFOLIO



** i.MX 93 and i.MX 8ULP are supported with TensorFlow Lite (Cortex-A) and TensorFlow Lite Micro (Cortex-M33)

*** Additional support for devices not listed can be available or requested

eIQ® MACHINE LEARNING ENVIRONMENT

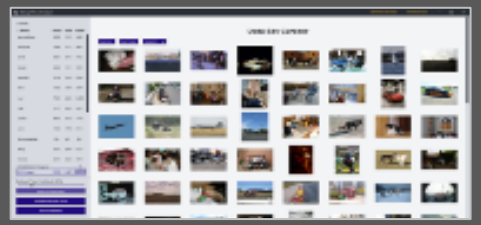
Embedded Developers

Data Scientists

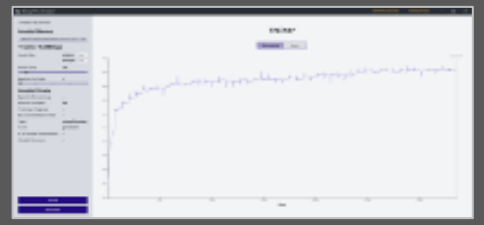
ML Experts

eIQ Marketplace

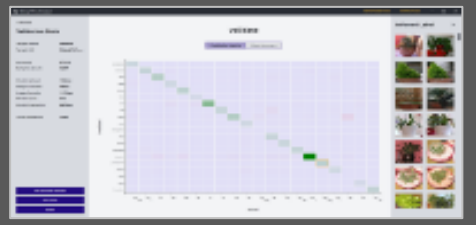
eIQ Toolkit



Data Labeling , Curation



Model Conversion Training, Optimization, Quantization



Model Validation, Profiling

eIQ Pipelines

AUDIO / VOICE

VISION

ANOMALY DETECTION

App SW Packs

STATE MONITOR

IDENTITY RECOGNITION

PERSON DETECTION

and more ….

From MCUs

SCALABLE COMPUTE

To Apps Processors

eIQ® ML Software Development Environment

Embedded Developers

Data Scientists

ML Experts

Extensible **workflow tools** for dataset management, model training, optimization, deployment, and profiling

eIQ Toolkit

eIQ Portal

eIQ Marketplace

Bring Your Own Data Workflow

Data Curation | Model Selection | Model Training, Optimization, Quantization | Model Validation

Bring Your Own Model Workflow

Solutions and Services from NXP and Partners

- ML applications
- Optimized models
- Optimization tools and modules
- Development tools
- Datasets
- Training
- Sensor solutions

Applications running on EdgeVerse processors

eIQ Pipelines

AUDIO / VOICE | VISION | TIME SERIES

STATE MONITOR | IDENTITY RECOGNITION | PERSON DETECTION

and more ….

App SW Packs

Inference engine support for compute engines (CPU, NPU, GPU, DSP) available on NXP MPU and MCU

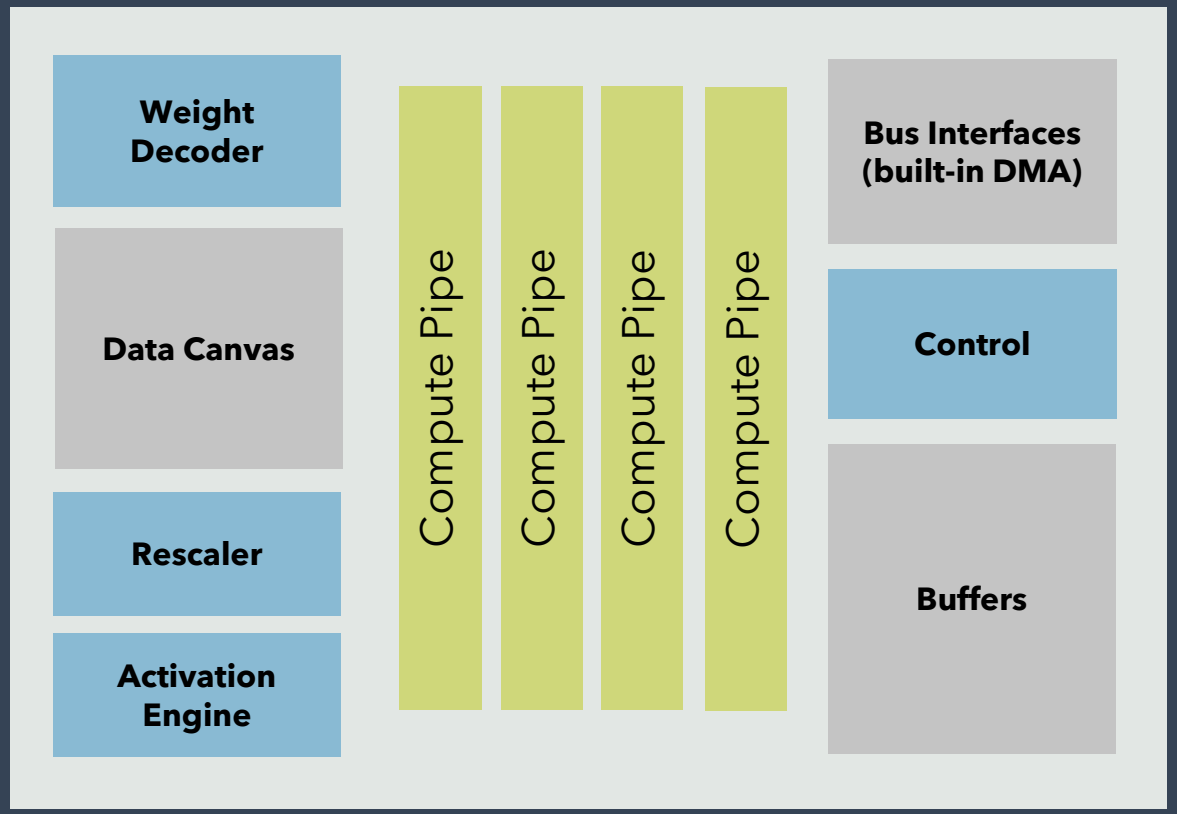
eIQ Inference

eIQ inference with…

TFLite for Microcontrollers → Arm® Cortex®-M, DSP, eIQ Neutron NPU

TFLite → Arm Cortex-A, GPU, DSP, NPU, eIQ Neutron NPU

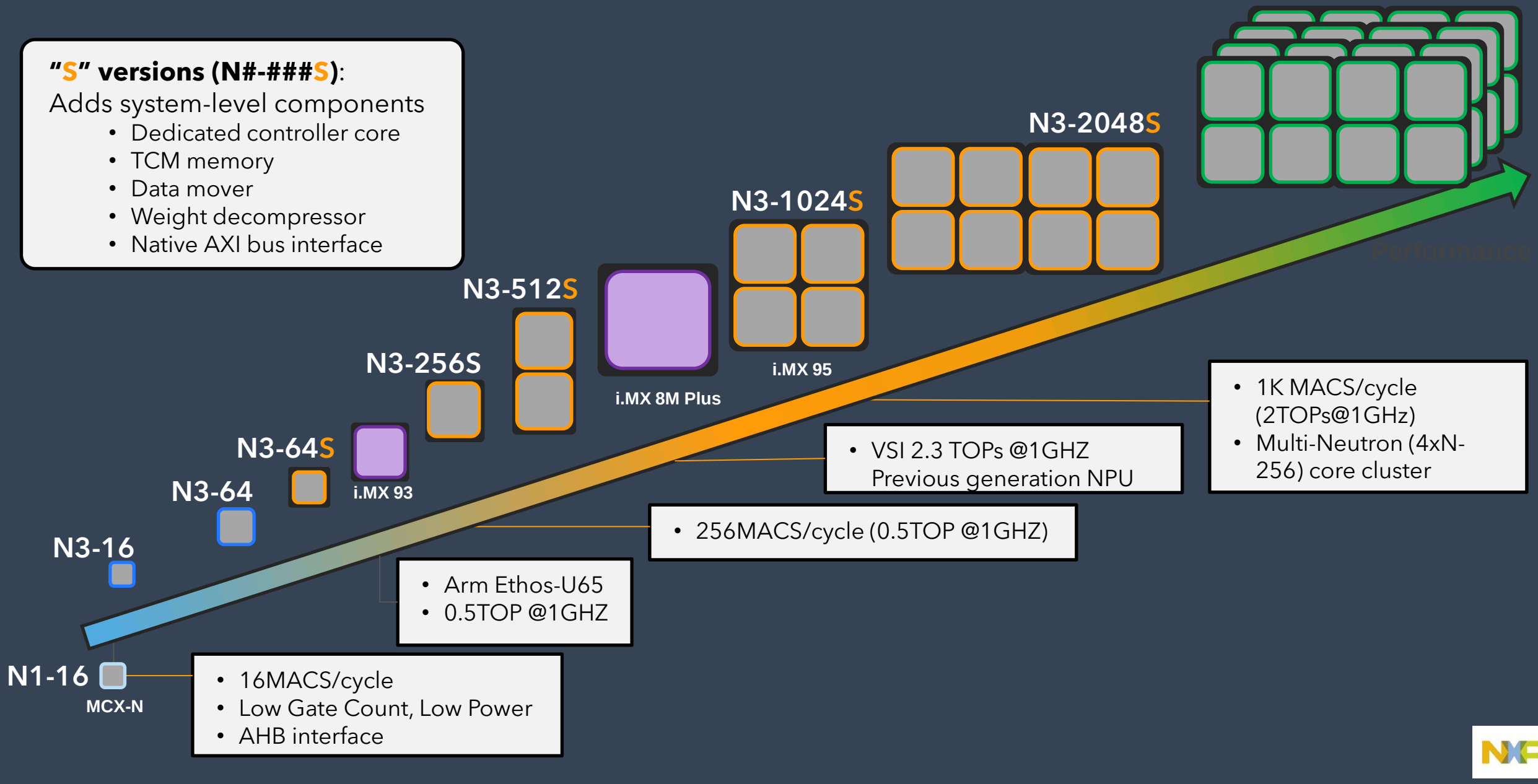
NXP eIQ Neutron NPU Accelerator



Single Architecture With Great Scalability

- Optimized for performance and power efficiency
- ML solution development support with eIQ® ML SW Development Environment
  - Supports major NN structures (CNN, MLP, RNN, LSTM, TCN, and more)
- Internal development provides flexibility to tune solution to better meet our customer needs and the ability to provide ongoing support and generational improvements for changing applications and operator support needs
- Hardware scales from performance efficient 32 Ops/cycle to 4k Ops/cycle and beyond for portfolio coverage with a single architecture, and potential to provide future expansion
- Software support is unified over multiple generations and device portfolio, creating consistent enablement and support solutions for our customers

SCALABLE ARCHITECTURE TARGETING THE VARIOUS DOMAINS



INDUSTRY AWARD WINNING eIQ SOFTWARE AND eIQ NEUTRON NPU HARDWARE

Embedded Computing Design, Best in Show Award at Embedded World:

AI & Machine Learning:

NXP eIQ Machine Learning Software Development Environment

Industry Recognition for our eIQ SW Enablement and our first silicon with eIQ Neutron NPU

MANAGE COMPLEXITY & TTM: DIGITAL TWINNING AND SW DEFINED VEHICLE

DRIVEN BY UBIQUITOUS CONNECTIVITY, CLOUD-/DATA-INFRA WITH CONTINUOUS LEARNING AND STANDARDS DRIVEN HW /SW PLATFORMS

CLOUD
CONNECTIVITY

SOFTWARE
PLATFORM

SOFTWARE

HARDWARE

HARDWARE
PLATFORM

INTELLIGENT EDGE SOFTWARE

INTELLIGENT EDGE

DATA SOURCES
CAMERA
RADAR
LiDAR
GPS
IMU
OTHER SENSORS

TERABYTES OF DATA/VEHICLE/DAY

VEHICLE PROCESSING PLATFORMS

DATA STREAM FROM VEHICLE

OVER-THE-AIR (OTA) SOFTWARE UPDATE

TWIN IN THE CLOUD

RELEVANT AND WIDE-RANGING DATA

MASSIVELY SCALABLE STORAGE AND COMPUTE

THE CONNECTED VEHICLE DATA LIFECYCLE

1 INGES

2 ENRICH, ALALYZE, STORE

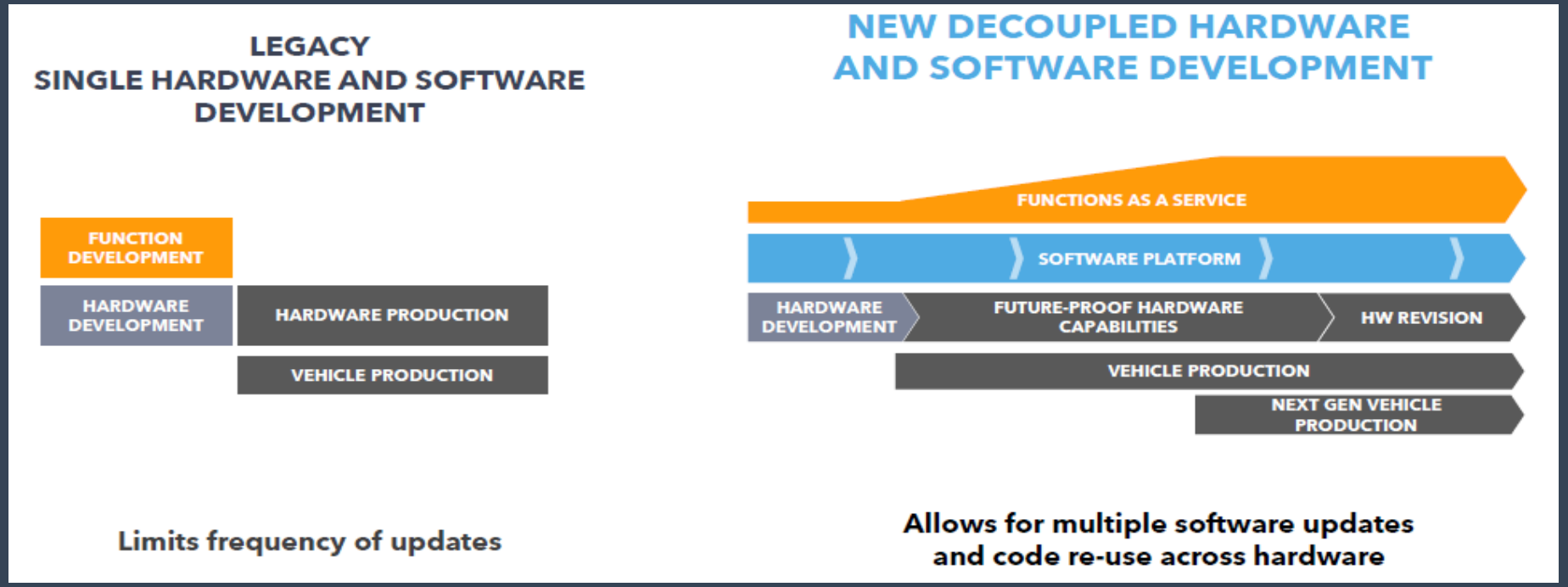
3 LEARN & DREAM

4 DEPLOY

DEPLOY SOFTWARE ML MODEL UPDATES TO VEHICLES

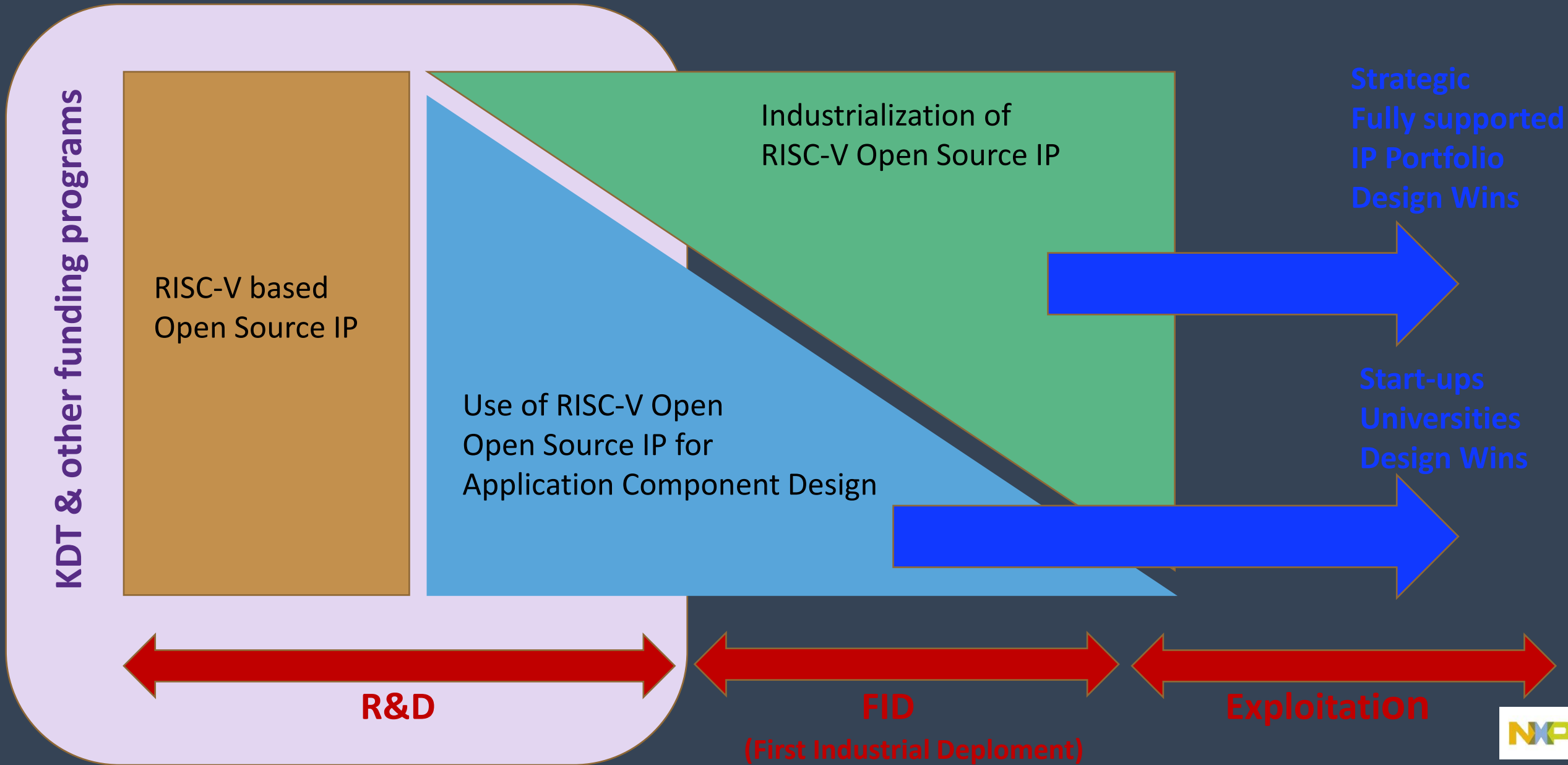
CONTINUOUSLY MONITOR DIGITAL TWINS AND UPDATE ML MODELS

DIGITAL TWIN AND SERVICE ORIENTED ARCHITECTURE FOR THE VEHICLE OF THE FUTURE , ENABLED BY STANDARDS BASED HW/SW PLATFORMS

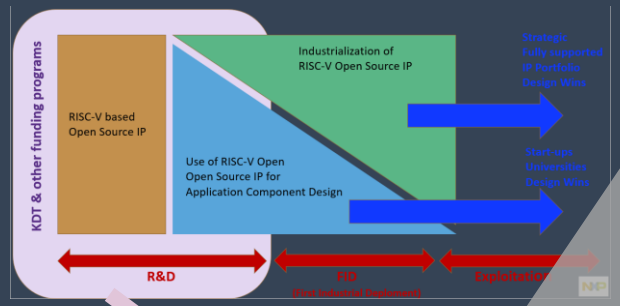


"Sw defined vehicle"

EU STRONGLY DRIVING OPEN HW/SW RISC-V IP AND PLATFORMS



EU FOCUS TOPICS IMPLEMENTATION PLAN (PRELIMINARY CONSIDERATIONS)



FOCUS TOPIC 9
Scalable Software-to-Silicon Creation Flow

FOCUS TOPIC 8
System Software Ecosystem for high assurance

FOCUS TOPIC 7
SoC building blocks libraries

FOCUS TOPIC 6
Verified re-usable die-to-die interfaces & chiplets technology

FOCUS TOPIC 5
Deterministic, verified and certifiable interconnects

FOCUS TOPIC 4
Economic and social aspects of open source hardware innovation

FOCUS TOPIC 3
Governance

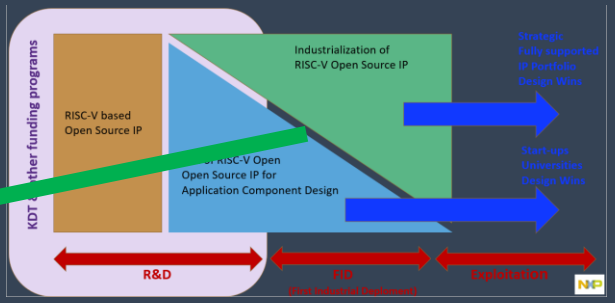
FOCUS TOPIC 2
Open-source methodologies, models & tools

FOCUS TOPIC 1
Advanced RISC-V Processor / Multicore

EO9 EO8 EO7 EO6 EO5 EO4 EO3 EO2 EO1

2023 2024 2025 2026 2027 2028 2029 2030

..... AND INDUSTRY JOINING FORCES



SIGN IN / UP

SYSTEMS

The Register

Big chip players join forces to form another RISC-V venture

Initial drive starts in Germany, pushes automotive blueprints

Dan Robinson

Fri 4 Aug 2023 // 16:29 UTC

The RISC-V open instruction set architecture got a boost today after it emerged that chip giants are coming together to jointly invest in a company to develop reference architectures based on the standard.

The new entity will be formed in Germany with investment from Infineon Technologies, Qualcomm, NXP Semiconductors, Bosch, and Nordic Semiconductor, with the aim of speeding up "the commercialization of future products based on the open-source RISC-V architecture."

If this sounds a bit vague, it is because the company's formation is subject to regulatory approvals in various jurisdictions, and so at this stage the founding corporations are unable to add any further detail about how much investment is involved, when it is expected to begin operations, or even what the company will be called.

What we do know is that this will not be a chip manufacturing operation, but will focus on the creation of reference designs to help increase the adoption of the RISC-V architecture. The aim is to establish the company as a single source for developing compatible RISC-V-based products.

SILICON SAXONY

THE HIGH-TECH NETWORK

COMPETENCES SERVICES MEMBERS EVENTS NEWS ABOUT US

Microelectronics

INFINEON, BOSCH AND NXP: LEADING SEMICONDUCTOR COMPANIES JOINTLY DRIVE RISC-V FORWARD

August 4, 2023. semiconductor companies Robert Bosch GmbH, Infineon Technologies AG, Nordic Semiconductor, NXP ® Semiconductors and Qualcomm Technologies, Inc. are jointly investing in a company that will enable the development of next-generation hardware to drive the adoption of RISC-V worldwide.

RISC-V

RISC-V: The Free and Open RISC Instruction Set Architecture

What is RISC-V ?

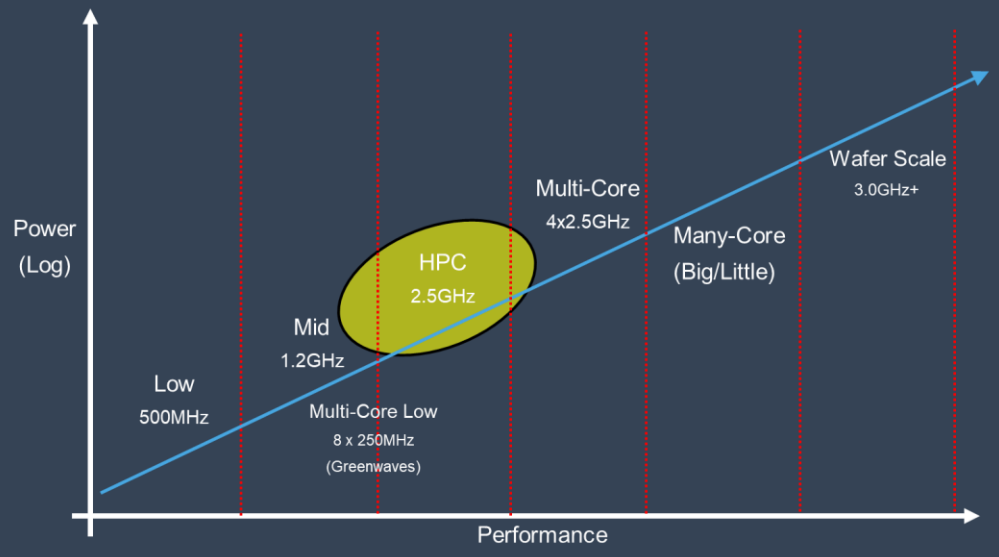
- Open standard instruction set architecture
- Provided under open-source licenses with no fees to use
- Initially designed for academic use and educational purposes
- Is the starting point for designing a HW processor in a certain process technology
- “RISC-V International’’ owns, maintains and publishes IP related to RISC-V – only specification, no implementation

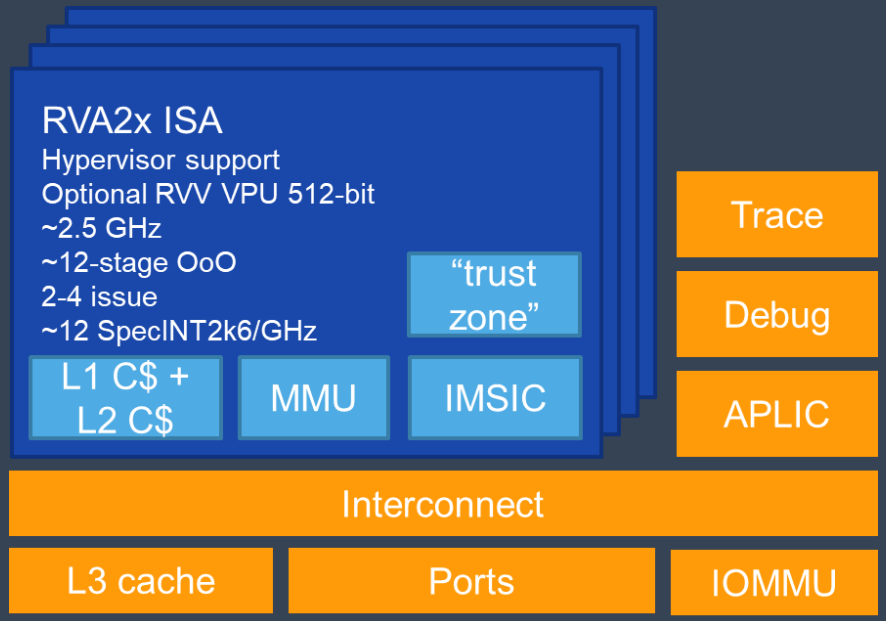
Chip companies join forces to form new RISC-V venture • The Register

Infineon, Bosch and NXP: Leading semiconductor companies jointly drive RISC-V forward - Silicon Saxony (silicon-saxony.de)

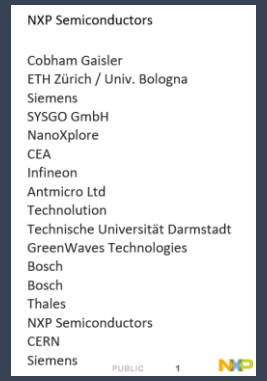
NXP

WORKGROUP AUTOMOTIVE HIGH PERFORMANCE COMPUTE PLATFORM



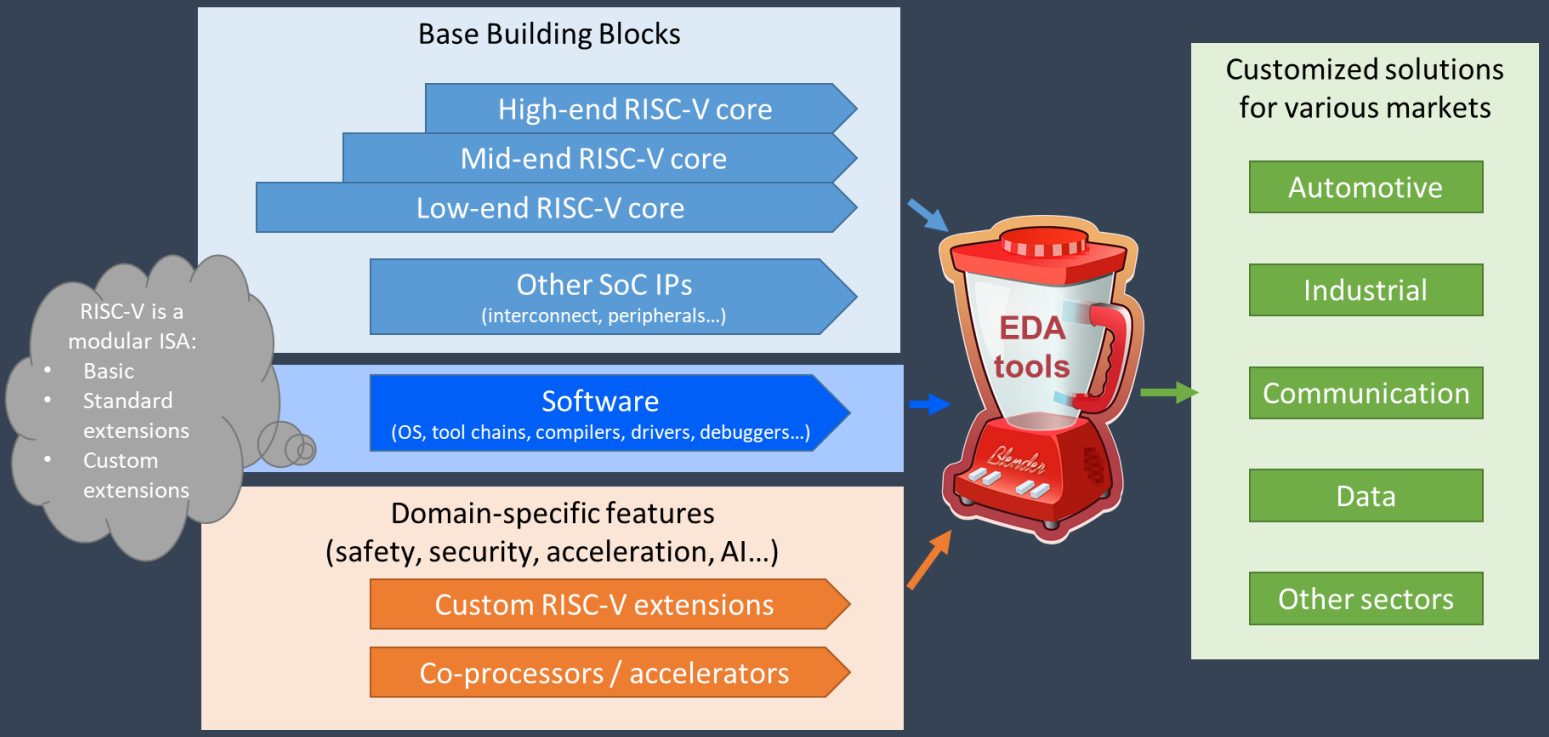


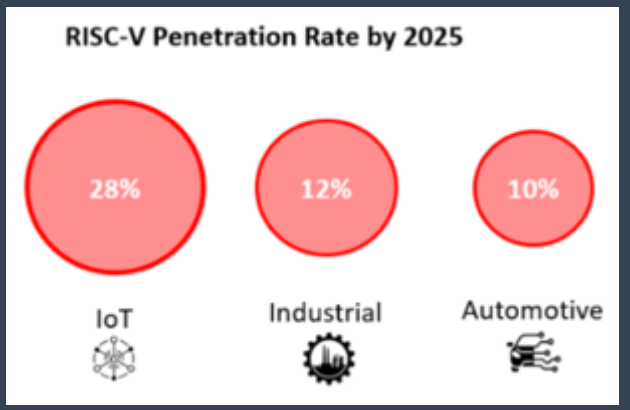
- European RISC-V and Open-Source Roadmap (*)
- Position Paper from our WG with Reference Platform Contents, Proposal for Instantiation and Questions to relevant stakeholders
- On-going work in KDT-projects TRISTAN & ISOLDE



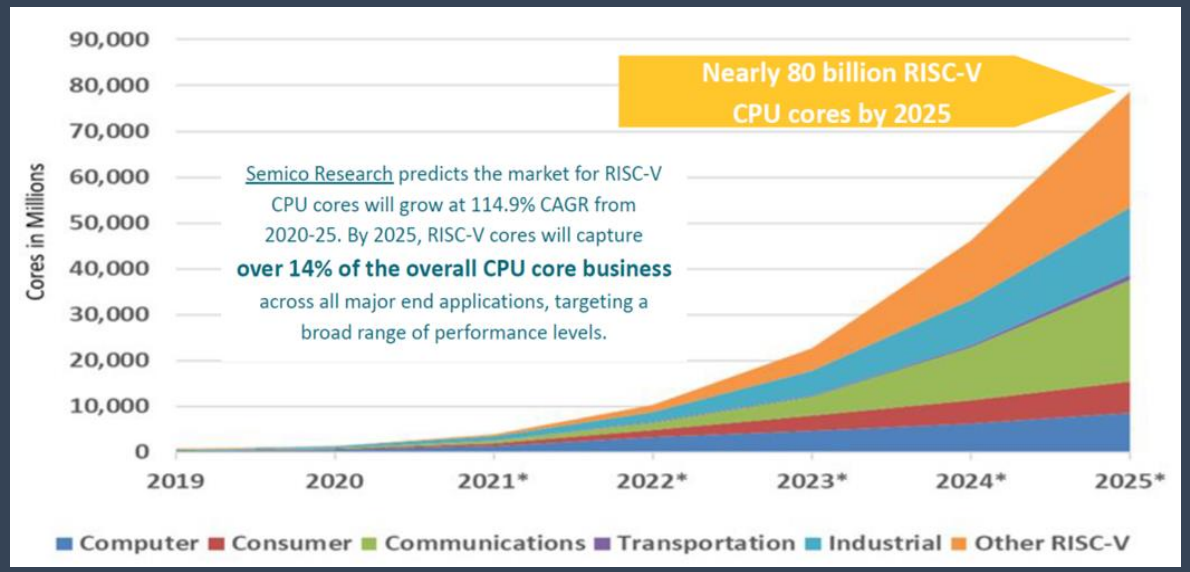
- Virtualization support
  - RV H Hypervisor support
  - MMU + IOMMU address translation/isolation
  - Advanced Interrupt Architecture (AIA):
    - APLIC (Advanced Platform-Level Interrupt Controller): Converting signal-based interrupts to MSIs
    - IMSIC (Incoming Message-Signaled Interrupt Controller): per core interrupt controller
- Functional safety:
  - Single core ISO26262 ASIL-B qualification
- Security:
  - ISO/SAE 21434 readiness/compliance

HOW THE MARKET IS ENVISAGED TO DEVELOP

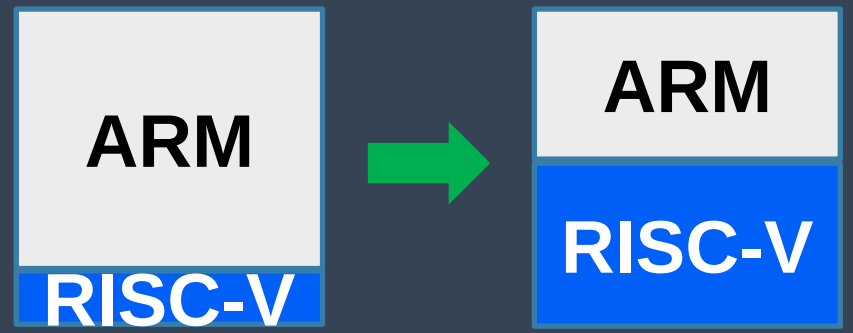




Source:https://www.counterpointresearch.com/riscv-semiconductor-ip-market-2025/

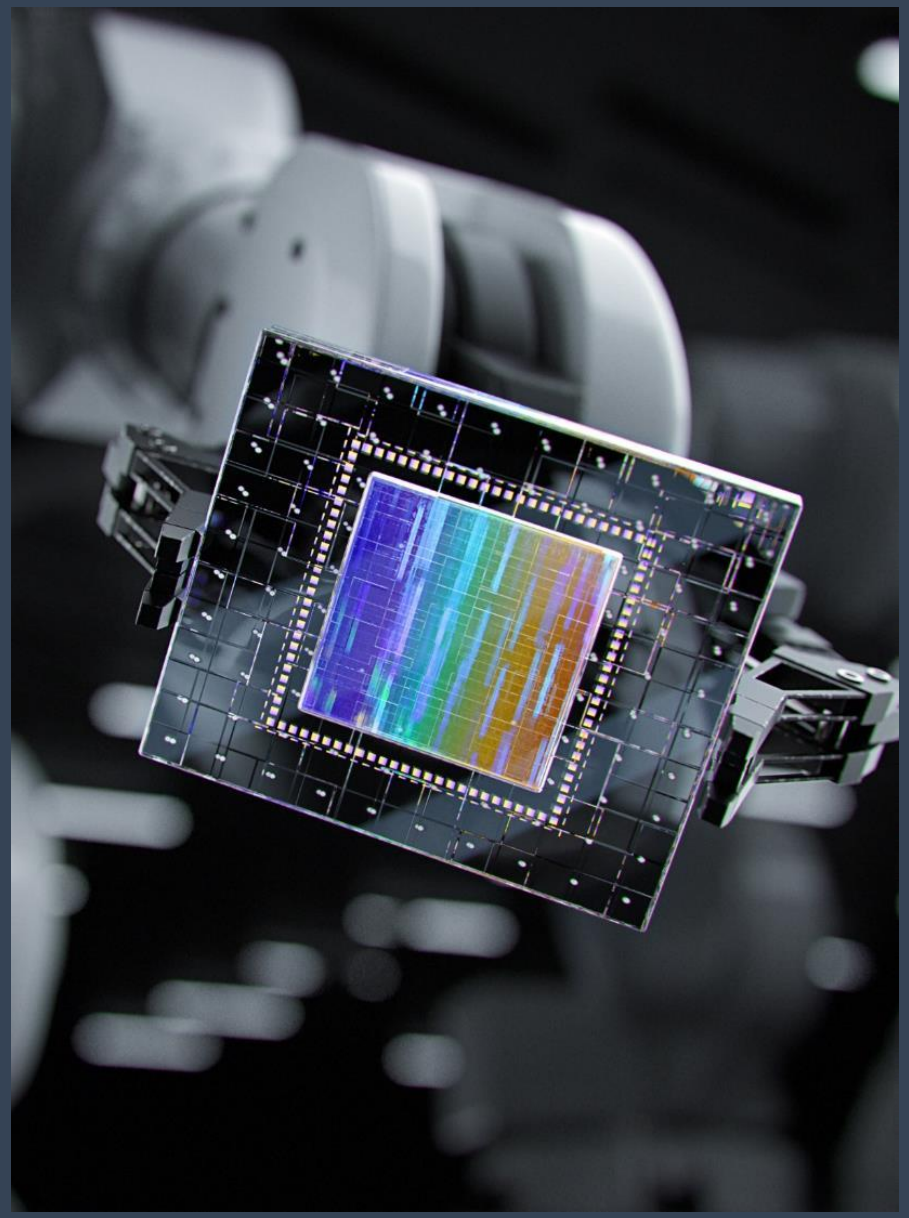


Towards a Better Balance



"23% of projects in both the ASIC and FPGA spaces incorporated at least one RISC-V processor." Source: Wilson Research Group Functional Verification, 2020

Conclusions

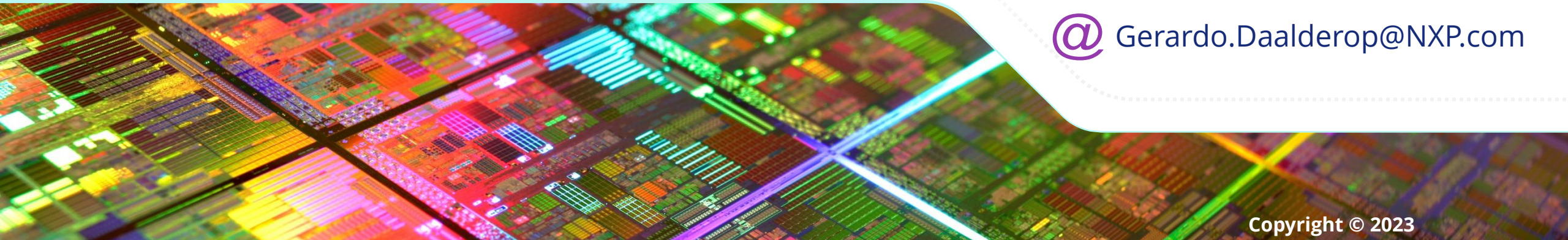


- The Edge offers significant opportunities for **growth and differentiation**; many possibilities for trade-offs between performance and other requirements
- **Ease of development** and **(open) reference-solutions / platforms** will be key to capture time-to market and raise the EU value-add
- **RISC-V and Open-Source** is seen as a driver for future platforms in a.o. automotive, exhibiting a modular scalable processor architecture with domain-specific extensions
- **Automotive architectures** are being re-considered/transformed

EDGE AI

Thank You

For your attention



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