Driving Next-Gen Edge AI Technologies Workshop

17 January 2024 Munich, Germany HiPEAC **Conference**

10:00 - 11:00 Session 1: Edge AI Concepts and Challenges

- *Edge AI trends and engineering principles applied to micro, meta, and end-to-end AI system verification, validation, and testing*, Ovidiu Vermesan (SINTEF)
- *The road to edge AI system benchmarking from requirements and robust modelling for verification till system validation and testing*, Mario Diaz Nava (STMicroelectronics)
- *Benchmarking neuromorphic computing systems*, Andrea L. Dunbar (CSEM)

11:00 – 11:30 Coffee/Tee Break

11:30 – 13:00 Session 2: Metrics and Tools

- *Advancing neuromorphic computing with NeuroBench*, Bernhard Vogginger (TU Dresden)
- *NeurIO: A Python library for deployment on edge devices*, Simon Narduzzi (CSEM)
- *SENECA: Lessons learned from architecting and building a fully digital neuromorphic processor*, Manolis Sifalakis (imec)

12:30 – 13:00 Panel discussion (Moderator: Manolis Sifalakis - imec)

13:00 – 14:00 Buffet Lunch

14:00 – 15:30 Session 3: Algorithms and Application

- *Ultra-efficient on-device object detection on AI-Integrated smart glasses with TinyissimoYOLO*, Michele Magno (ETHZ)
- *Evaluating federated learning for malware detection at the edge*, George Xenos and Dimitrios Serpanos (CTI and University of Patras)
- *Self-powered vibro-acoustic micro-edge condition monitoring: journey and roadmap*, Clemens Saur (Neurocontrols)

15:00 – 15:30 Panel discussion (Moderator: Fabian Chersi - CEA)

15:30 – 16:00 Coffee/Tee Break

16:00 – 18:00 Session 4: System-level Benchmarking

- *Automated software in the loop (SIL) and hardware in the loop (HIL) benchmarking*, Tim Llewellynn (Bonseyes)
- *Comparing implementations of a small CNN on commodity hardware*, Frédéric Pétrot (Université Grenoble Alpes)
- *At-the-edge AI acceleration on FPGAs, from CNNs to SNNs*, Paolo Meloni (Università degli Studi di Cagliari)
- *Accelerating intelligent threat detection at the Edge: CPU, GPU, or FPGA?*, Abdelghani Bourenane (Scuola Superiore Sant'Anna)
- *REBECCA: Full stack HW and SW for RISC-V with tightly-coupled hardware accelerators on the edge*, Ioannis Papaefstathiou (Exapsys)

17:30 – 18:00 Future steps panel discussion (Moderators: Andrea L. Dunbar – CSEM, Mario Diaz Nava – STMicroelectronics, Ovidiu Vermesan - SINTEF)

18:00 End