EDGE AI Newsletter

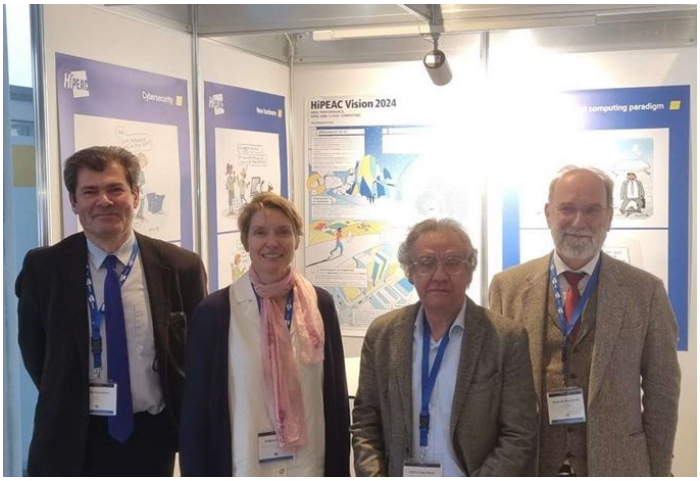
Volume 5, Issue 1
April 2024

Driving Next-Gen Edge AI Technologies Workshop, 17 January 2024, Munich, Germany

The "Driving Next-Gen Edge AI Technologies" workshop was arranged on 17 January 2024 as a full-day event at the HiPEAC 2024 Conference in Munich, Germany.

The event was co-organised by large-scale Chips JU EdgeAI, ANDANTE, REBECCA, CLEVER, NEUROKIT2E, and Horizon Europe dAIEDGE projects to exchange ideas for providing a set of reference comprehensive benchmarking solutions by bringing together a diverse community of experts, researchers, and industry leaders to collectively tackle the intricacies of benchmarking in edge AI.

The workshop addressed the latest developments in the implementation of edge AI technologies and presented and discussed the advances in intelligent embedded devices across the edge AI computing continuum from micro- to deep- and meta-edge.



One of the workshop's highlights was the exploration of reliable verification, validation, testing and comprehensive benchmarking solutions for edge AI, areas expected to redefine the dependability and trustworthiness of future edge AI systems. The discussions focussed on leveraging different techniques, methods, and gaps for rapid deployment of engineering principles to address the development of standardised edge AI benchmarking solutions were particularly enlightening. The hands-on approach taken by the speakers allowed the audience to navigate between the theoretical concepts and the practical examples, fostering a dynamic learning environment.

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What differentiated the workshop from similar events was its focus on the challenges, technology gaps and real-world application requirements. The comprehensive nature of the workshop provided a holistic view of verification, validation, testing and comprehensive benchmarking for edge AI components and systems, bridging the gap between theory and practical implementation.

124 participants from 80 institutions and 22 countries registered for the workshop, which included 14 presentations and 3 panel discussions.

The panel discussions addressed lessons learned from the speakers' experience with edge AI benchmarking solutions, and all highlighted the importance of research and innovation for developing edge AI benchmarking solutions.

The Chips JU EdgeAI project was the main organiser, with several project beneficiaries (SINTEF, STMicroelectronics, Università degli Studi di Cagliari, NEUROCONTROLS, CEA, Institut polytechnique de Grenoble) participating and presenting during the workshop.

EDGE AI Newsletter

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Driving Next-Gen Edge AI Technologies Workshop - Impressions

Ovidiu Vermesan, Chief Scientist at SINTEF

"An enlightening workshop providing challenging thoughts on verification, validation, testing and benchmarking for edge AI components and systems. The discussions around these topics were exciting, generating edifying new ideas and valuable points from a diverse and dynamic audience."

Paolo Meloni, Associate professor at Università degli Studi di Cagliari

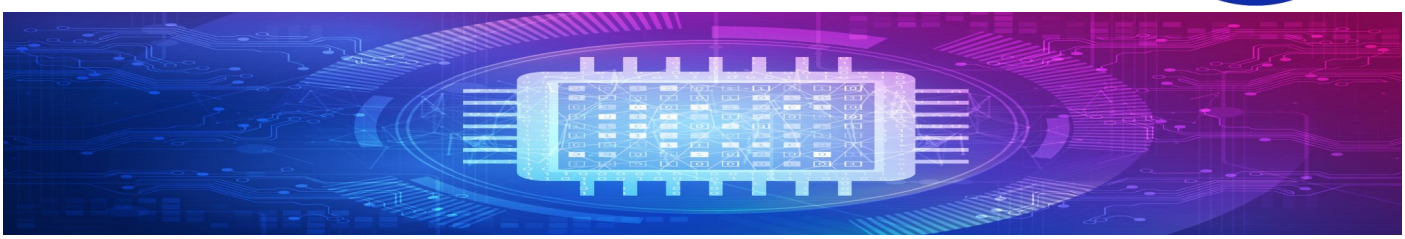
"The workshop was an inspiring blend of technical talks, covering not only how to develop, program, and connect edge-AI devices but also how to compare and validate solutions. It provided very important links to new benchmarking and simulation methodologies. I believe it was a great effort towards harmonizing a common vocabulary for the community involved in AI at the edge."

Clemens Saur, Managing Director at NeuroControls

"Great exchanges on scientific possibilities and down to earth practical industrial implementations. Pushing both State-of-the Science and shifting State-of-the-Art. Edge AI has a great future. NeuroControls will add to it self-powered vibro-acoustic micro–edge sensors merged with secure VHF Blockchain transactions."

Frédéric Pétrot, Professor at Université Grenoble Alpes

"The workshop covered many aspects of the challenges in Edge AI implementation and deployment. Benchmarking is critical for these topics, and we had many discussions on what to measure and how to do that in a fair and consistent way. Still many open questions, that is also the interest of sharing our experiences in such venues!



EDGE AI Newsletter

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Workshop on Design and Architectures for Signal and Image Processing, 18-19 January 2024, Munich, Germany

The 17th edition of the Workshop on Design and Architectures for Signal and Image Processing (DASIP) was held in conjunction with the 19th HiPEAC Conference in Munich, Germany, on January 18-19, 2024. The workshop provided an inspiring international forum for the latest innovations and developments in the fields of leading signal, image, and video processing and machine learning in custom embedded, edge, and cloud computing architectures and systems.

This year's edition focused, as main discussion topics, on specialized hardware architectures for signal and image processing, optimization approaches for efficient deployment of signal and image processing applications, and digital signal processing design for reconfigurable systems. The contributions presented during the workshop - nine papers from twelve different countries accepted for oral presentation -, were selected through a thorough review process, thanks to an outstanding international Technical Program Committee.

The Best Paper Award was granted to Chilankamol Sunny (Indian Institute of Technology Palakkad), Satyajit Das (Indian Institute of Technology Palakkad), Kevin Martin (Lab-STICC - Université de Bretagne-Sud), and Philippe Coussy (Lab-STICC - Université de Bretagne-Sud) for their paper entitled "Standalone Nested Loop Acceleration on CGRAs for Signal Processing Applications".

EDGE AI Newsletter

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April 2024

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The event was opened by the inspiring keynote held by David Gonzalez-Arjona, from GMV Aerospace & Defence (Spain). It addressed the challenges to be faced for effectively exploiting edge computing in space avionics, where remote, autonomous, and fault-tolerant processing capabilities are paramount due to discontinuous communication with the ground.

The future challenges in the field of embedded AI for image and signal processing were also discussed during a valuable discussion panel, held by Andrea Pinna, from Sorbonne University (France), Marek Gorgon, from AGH University of Science and Technology (Poland), and Paolo Meloni, from the University of Cagliari (Italy).

DASIP is a long-running event that has been held annually since 2007, with the contribution of an international Steering Committee, gathering members from multiple research groups from Europe and Canada. This year's edition was co-chaired by Tiago M. Dias from the ISEL - Lisbon School of Engineering from Politécnico de Lisboa (Portugal), and Paola Busia from the University of Cagliari (Italy).

We are planning to organise the 18th edition of DASIP in conjunction with the 20th HiPEAC conference in Barcelona, Spain. Please visit our website - https://dasipws.github.io/ - and consider contributing to the workshop.

EDGE AI Newsletter

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April 2024

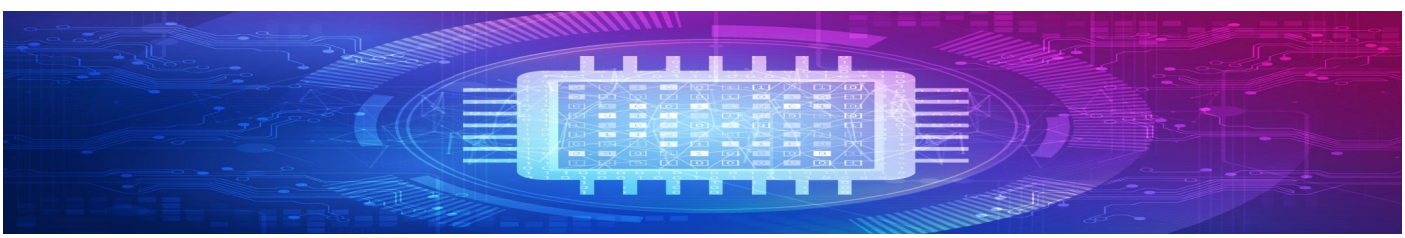
Tech Talk 2024 Strategic Event, 8-9 February 2024, Barcelona

EdgeAI project joined the Tech Talk 2024 Strategic Event in Barcelona!

The two-day Tech Talk "Navigating the Convergence of Ecosystems" organised by AVL List, STMicroelectronics, NXP, SINTEF, Infineon, and Teraglobus, provided a deep dive into the interconnected world of technology convergence.

The Tech Talk featured a unique format of "fishbowl discussions", where attendees actively engaged in conversations on a variety of cutting-edge topics, including:

- The emergence of human-like AI in everyday interactions.
- The crucial role of semiconductors and software: From power electronics and 6G to RISC-V-powered solutions for Software Defined Vehicles and edge AI.
- The impact on society and citizens: How are these technologies influencing our lives and the world around us? What are the potential benefits and challenges we need to consider?



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April 2024

Tech Talk 2024: Did you miss it? Check some of our photos!

Did you miss the Tech Talk 2024 Strategic Event?

Don't miss out on what's next!

Follow us on social media for updates on future events, and even more exciting news!

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https://edge-ai-tech.eu/

EdgeAI

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EdgeAI Key Facts

Start: 01 December 2022

Duration: 37 months

Budget: 35,43 M€

Coordinator: SINTEF AS

Consortium: 48 partners

Consortium

SINTEF, Infineon, ams OSRAM, SoftwareCUBE, TU Wien, imec, NXP, GNT, NEURO Controls, COGNITION FACTORY, IMST, Universität zu Lübeck, scm group, ST life.augmented, Vranken Pommery, TECHNEXT, cea, Grenoble INP UGA, Université de Reims Champagne-Ardenne, cnrs, Université Polytechnique Hauts-de-France, Χαροκοπειο Πανεπιστημιο Harokopio University, HTS High Technology Systems, Intelligent Machines IoT & Cyber Physical Systems DeepSensing S.R.L., Xtremion, Università degli Studi di Cagliari, Alma Mater Studiorum Università di Bologna, Università degli Studi di Milano, Elektronikas un datorzinātnu institūts Institute of Electronics and Computer Science, signify, Technolution, almende, TU/e, Fredrikstad energi, NxtEnergy, PROLUX, nxtech, itml innovation applied, Convergence, SynSense

Disclaimer

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This project has received funding from Chips JU under grant agreement No 101097300. The Chips JU receives support from the European Union's Horizon Europe research and innovation program and Austria, Belgium, France, Greece, Italy, Latvia, Netherlands, Norway.